COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

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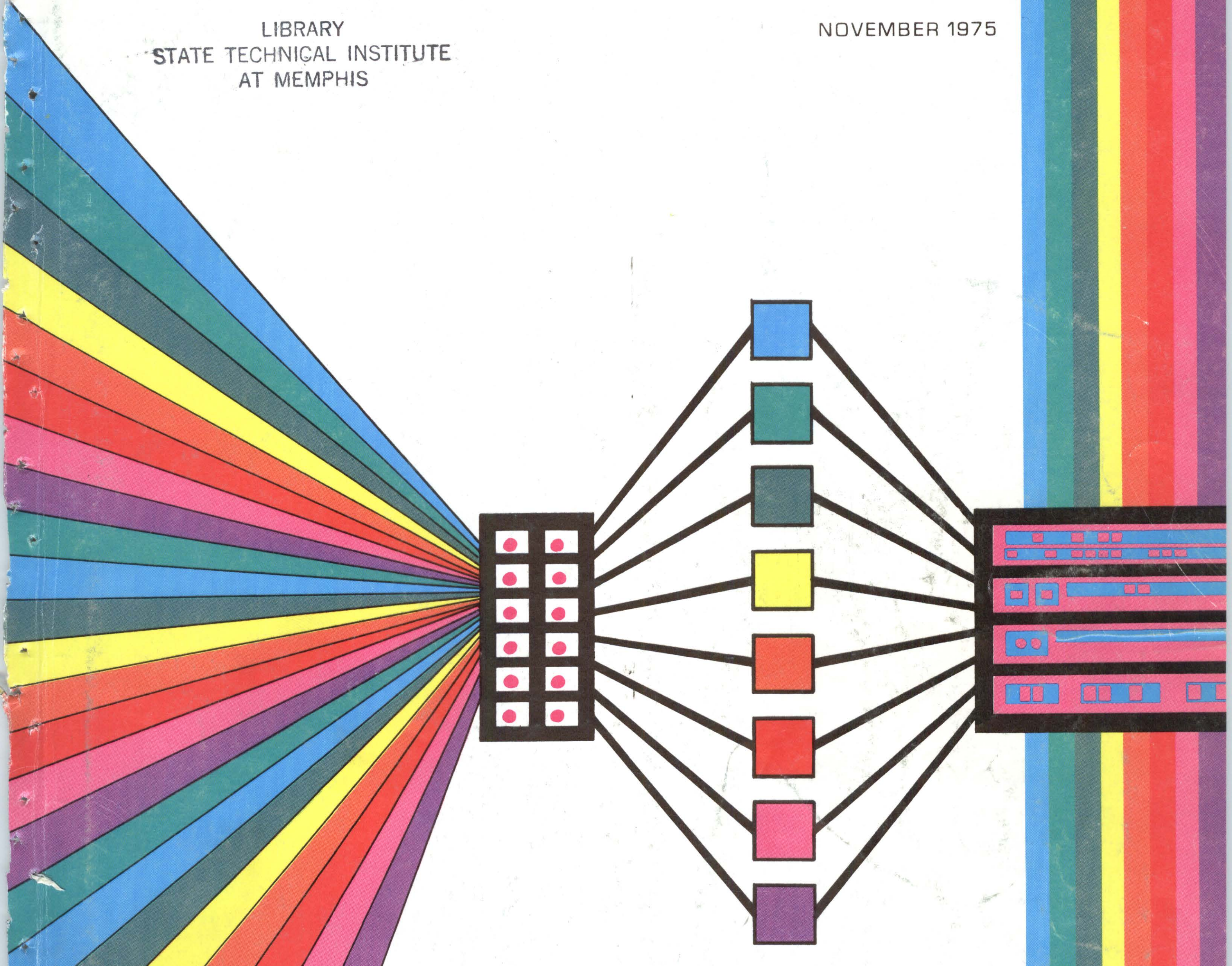
NOVEMBER 1975



A NEW APPROACH TO NETWORK STORAGE MANAGEMENT

OPERATOR'S CONSOLE CONSIDERATIONS
IN MICROPROCESSOR SYSTEM DESIGN

UNDERSTANDING CYCLIC REDUNDANCY CODES

Where other data terminal systems grow old, this one is designed to simply grow.

The Teletype® model 40 is the data terminal system to start with because it's completely modular, and is designed to grow as your needs grow.

The display, operator console, printer and controller modules form the heart of the model 40 system and permit a variety of configurations to suit your application.

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For instance:

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3. For options, we offer our own ferrite heads which expand performance life by a factor of 5.
4. For simplicity of customer electronics, we offer 7 and 9 track NRZ1 and PE formatter and popular mini-computer controllers.

We've kept the features that makes Series 9000 the best. Features such as 7 and 9 track, 800 NRZ1, 1600 PE or 800/1600 NRZ1/PE. We still have our front-accessible off-line test panel; our marginal skew check; threshold scanning to automatically compensate for drop-outs or drop-ins; our Read-After-Write shortened skew gage; simplified tape path and quick-release hubs.

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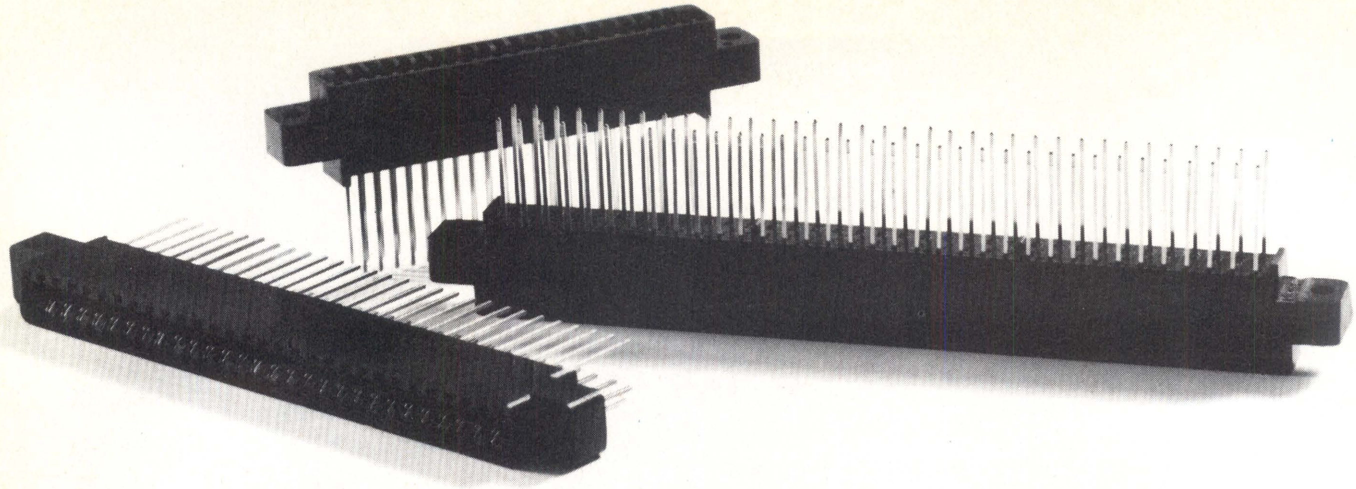

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CIRCLE 3 ON INQUIRY CARD

THE
MAGAZINE
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ELECTRONICS

COMPUTER DESIGN

NOVEMBER 1975 • VOLUME 14 • NUMBER 11

FEATURES

DEPARTMENTS

BPA CIRCULATION OVER 55,000

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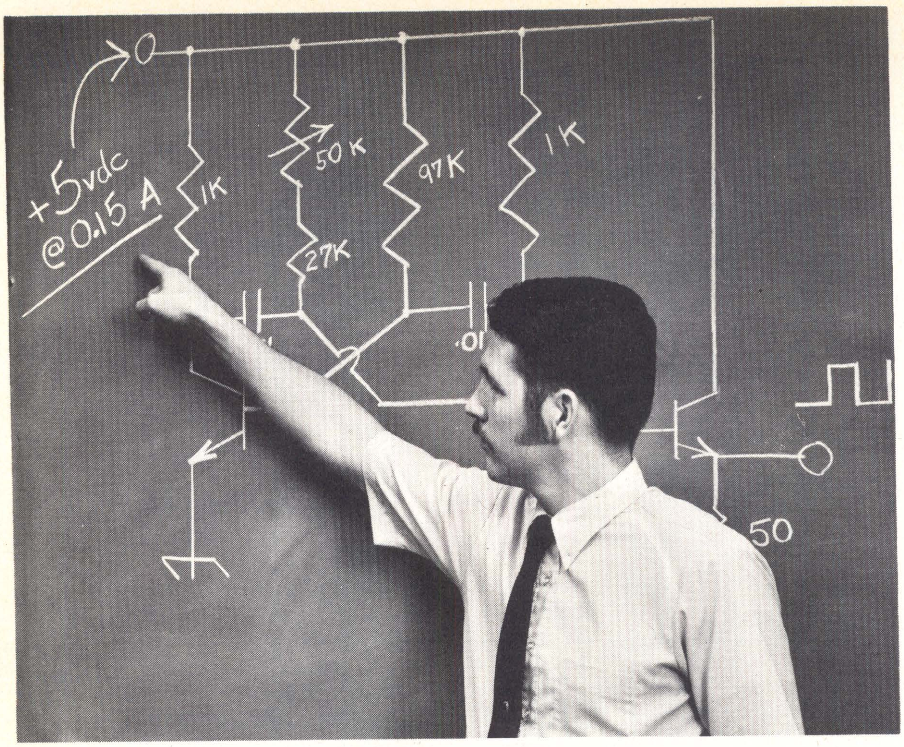

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LETTERS TO THE EDITOR

To the Editor:

I read Mr Wulfinghoff's article on small computers ["Market Factors Portend Design Changes in Small Computers," Aug 1975, pp 81-87] with considerable interest. I think the evolutionary trends he describes are well under way. However, there are some possibilities and variations in the way things could go that weren't really touched on.

Very small computers could become memory-limited, but I would expect futher cost reductions (at the system level) to be more I/O-limited—especially if the memory conservation techniques he proposes work out.

If we think in terms of the "orthodox" way of using microprocessors (if such a word can be used yet), I/O is no problem because the computer exists to serve some machine to which it is wired, not the other way around. He seems to be talking about data processing, though. This means the handling of more information than is likely to fit in main memory in the foreseeable future. There have to be ways of getting it to and from people, and of storing it outside main memory and retrieving it again. This sounds like a requirement for conventional I/O devices; yet to crack open large markets, it's questionable whether conventional solutions can ever be implemented cheaply enough.

A lot could be done with unconventional I/O devices. For instance, a terminal could be packaged like a calculator, with the same kind of display and about as many keys. It might even *be* a calculator. However, it would have serial ASCII input and output, either current loop, or with an acoustic coupler with pull-out, stick-on transducers. With either a folding keyboard or a new one-hand configuration, it could even be fully alphameric and yet pocket-size.

However, with computers becoming smaller and better, intelligence could be added to anything. The standard office typewriter is a prime candidate. With a computer in it, it becomes a terminal and an editing device. A tape recorder could become a dictating machine, telephone answering machine with time code recorder and a variety of responses, or a sequential file processing device. A disc drive, drum, or CCD memory can be an automatic filing cabinet, accessed and updated from anywhere in a network of connected terminals. A TV becomes a display device with video overlay capabilities, capable of selecting desired information from a digital broadcast.

The real challenge would be in coming up with simple, standard software that would be as plug-compatible as the hardware. National standardization of many kinds of file and record formats would be a necessity, so that information from one machine could be sent to another.

The main idea, though, is to get away from the idea of a computer surrounded by peripherals, and instead think in terms of standard office machines that can process data and guide the machine through any series of operations it's physically capable of. Thus, machines would tend to have more multipurpose capabilities than they have now. Many offices might end up with less machinery, and it would do more. Information flows would be rearranged to avoid the necessity of having some of the more expensive mechanisms such as card punches and paper-tape readers. Expensive line printers would probably be replaced by online lookup of central files through pocket terminals or office typewriters. Separate teleprinters would probably disappear, as would such complex special machines as the MT/ST.

Each peripheral becomes an autonomous machine, whose functions are expanding by plugging in extra ROMs which would be products in themselves. A "data processing system" would exist only for the duration of a task, while the needed machines were in communication. The closest thing to a central computer would be the user's terminal controller, which would ask other machines for needed information and send results on their way. Yet it wouldn't be concerned with file management or attempt large processing jobs by itself. It would manage the sequencing of a job according to the user's key strokes, within its own capabilities and those of the other machines involved in the job.

I don't think the function of user programming is likely to be eliminated in the near future. However, as calculators come with more mathematical functions and architectural conveniences built in as time goes on, office machines will come programmed with more and more of the data processing jobs everybody does. I can envision office-supplies catalogs devoting dozens of pages to program plug-ins, customizing key-caps, and so on.

One of the attractive aspects of the growing use of microprocessors is that a wide variety of machines—production, office, and miscellaneous—are being run by something that has a common kind of I/O: the serial ASCII port. This raises the interesting possibility of having telemetry and remote control inherent in practically everything.

On that note I will leave it to others to consider the implications.

John A. Carroll
25 Evergreen Ave
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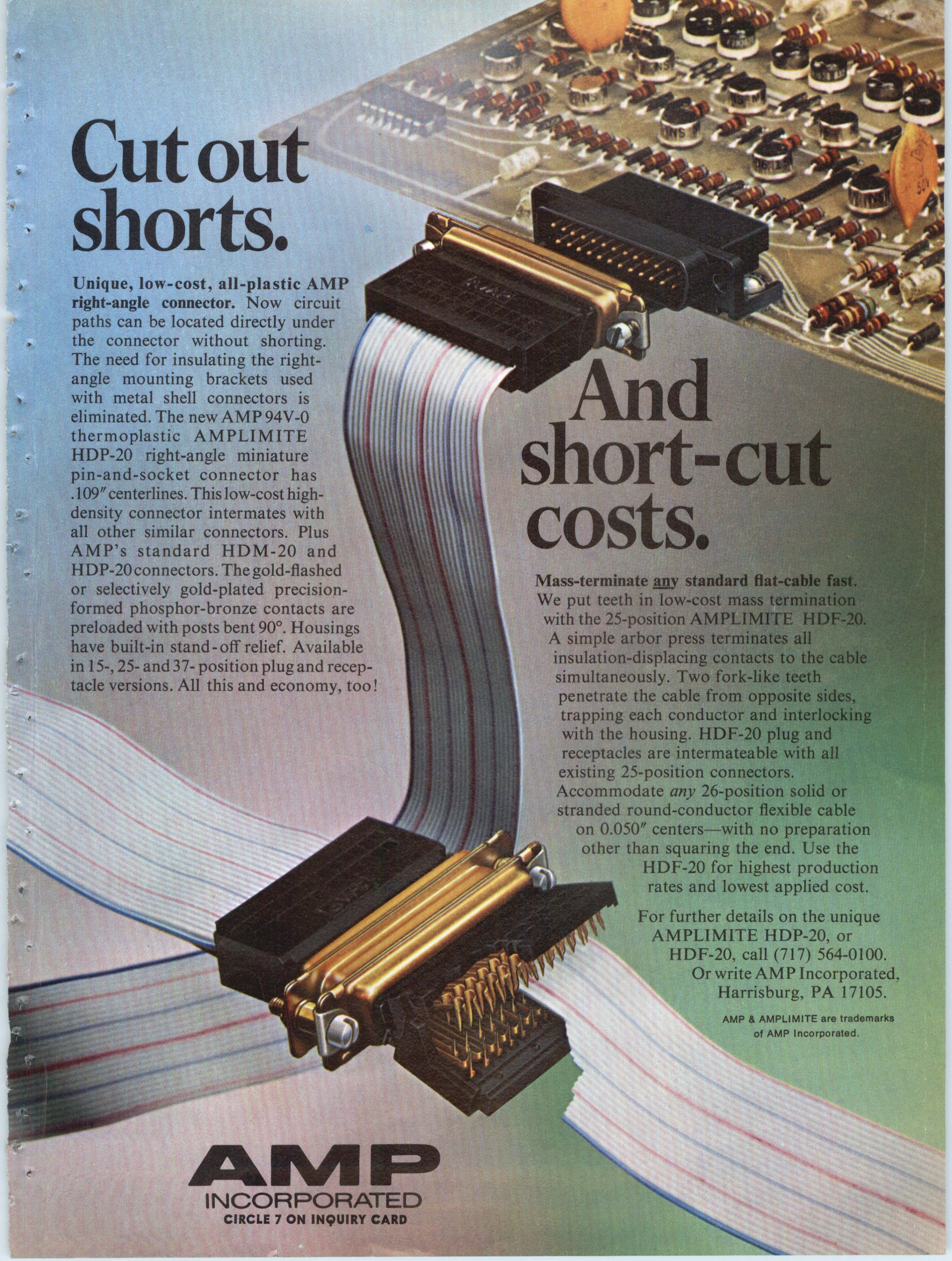

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For further details on the unique AMPLIMITE HDP-20, or HDF-20, call (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.
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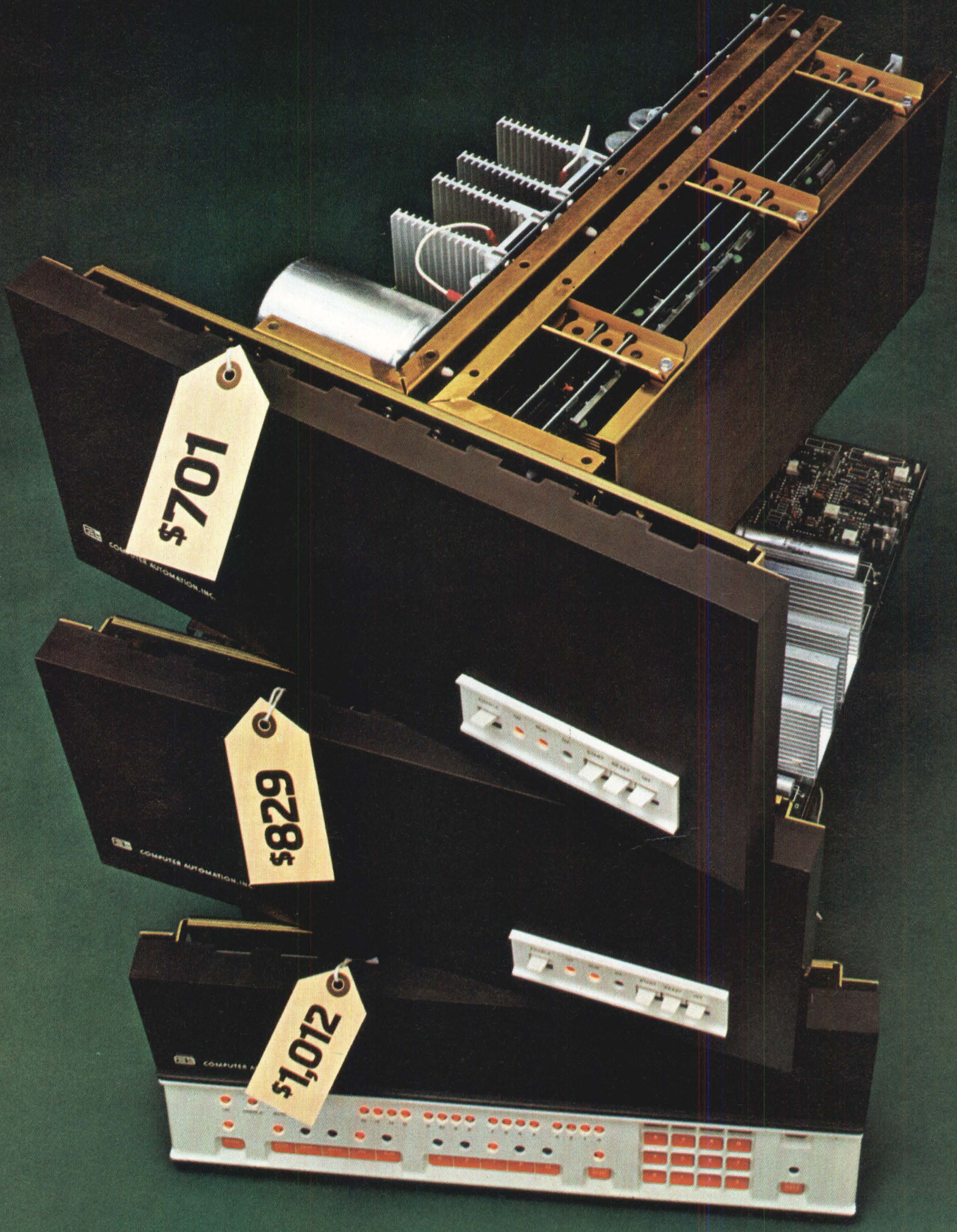

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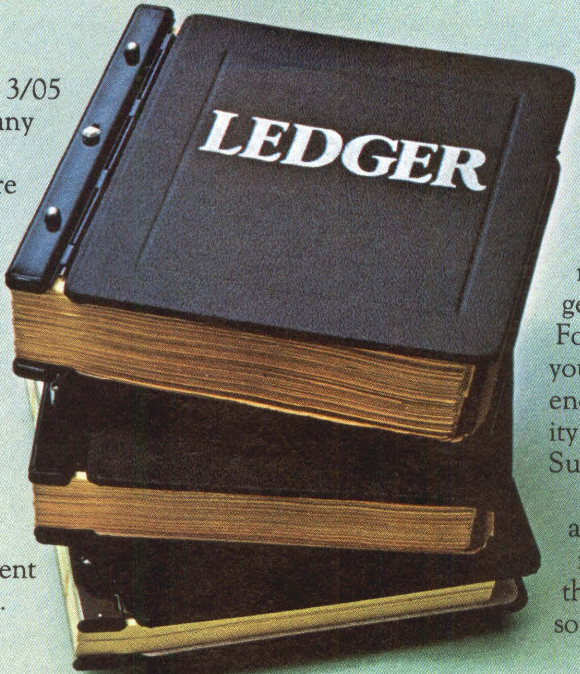

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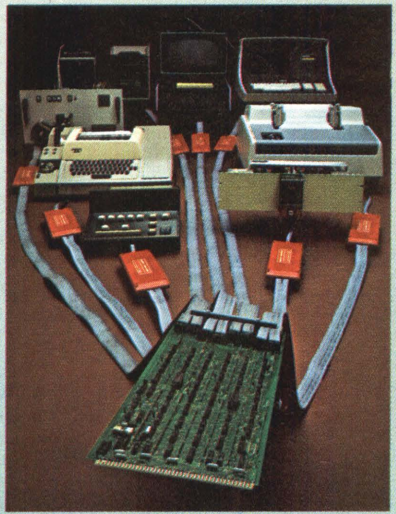

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CALENDAR

CONFERENCES

Dec 1-3—IEEE Internat'l Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. **Information:** Institute of Electrical & Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Dec 1-3—IEEE Nat'l Telecommunications Conf, Fairmont Hotel, New Orleans, La. **Information:** Institute of Electrical & Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Dec 9-12—21st Annual Conf of Magnetism and Magnetic Materials, Benjamin Franklin Hotel, Philadelphia. **Information:** Conf Chm, R. L. White, 124 McCullough Bldg, Stanford U, Stanford, CA 94305; or Local Conf Chm, B. Stein, Univac div of Sperry Rand, PO Box 500, Blue Bell, PA 19422

Dec 11-12—CECC/CEDPA (Calif Educational Computer Consortium/Calif Educational Data Processing Assoc) Joint Conf & Trade Show, International Hotel, Los Angeles. **Information:** Ellen Landers, Show Mgr, 1975 CECC/CEDPA, 17123 Chatsworth St, #10, Granada Hills, CA 91344. Tel: (213) 360-2786

Jan 15 (Houston, Tex), **Feb 17** (Fort Lauderdale, Fla)—Invitational Computer Conf. **Information:** B. J. Johnson & Assoc, 300 Otero, Newport Beach, CA 92660. Tel: (714) 644-6037

Jan 19-21—2nd Annual Sym on Computer Architecture, Fort Harrison Jack Tar Hotel, Clearwater, Fla. **Information:** Oscar N. Garcia, U of South Florida, College of Eng, Tampa, FL 33620. Tel: (813) 974-2581

Jan 20-23—Computer Soc of India Annual Conv, Hyderabad. **Information:** DVR Vithal, Prog Chm, CSI 75 Computer Grp, Tata Institute of Fundamental Research, Bombay 400 005, India

Jan 29-30—3rd Internat'l Congress on Computers in Industry, Hotel Hilton, Paris. **Information:** P. Daudier de Cassini, Institut d'Informatique et de Gestion, Insig-5, Rue Quentin-Bauchart, 75008 Paris, France

Feb 10-12—4th Annual ACM Computer Science Conf, Disneyland Hotel, Anaheim, Calif. **Information:** Assoc for Computing Machinery, 1133 Ave of the Americas, New York, NY 10036. Tel: (212) 265-6300

Feb 18-20—IEEE Internat'l Solid-State Circuits Conf, Sheraton Hotel, Philadelphia, Pa. **Information:** Institute of Electrical & Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Feb 18-21—IEE 2nd Internat'l Conf on Telecommunication Switching Systems, Kongresshaus, Salzburg, Austria. **Information:** Annemarie Cunningham-Swendell, Institution of Electrical Engineers, Savoy Pl, London WC2R 0BL, England

Feb 24-26—COMPCON 76 Spring, Jack Tar Hotel, San Francisco, Calif. **Information:** IEEE Computer Soc, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

Mar 2-4 (Boston), **Mar 9-11** (New York City), **Apr 13-15** (Chicago), **May 4-6** (Los Angeles), **May 11-13** (San Francisco)—CompDesign/76 Tour. **Information:** Jack Edmonston, The Conference Co, 797 Washington St, Newton, MA 02160. Tel: (617) 965-5800

Mar 4-6—ACM Conf on Programming Micro/Minicomputers, Delta Towers Hotel, New Orleans, La. **Information:** Association for Computing Machinery, 1133 Ave of the Americas, New York, NY 10036. Tel: (212) 265-6300

Mar 8-10—IEEE Conf on Industrial Electronics & Control Instrumentation (IECI '76), Sheraton Hotel, Philadelphia, Pa. **Information:** Institute of Electrical & Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Mar. 17-19—9th Annual Simulation Sym, Tampa. **Information:** Ira M. Kay, Southern Simulation Service, Inc, PO Box 22573, Tampa, FL 33622. Tel: (813) 839-5201

Apr 5-7—IEEE Region 3 Conf & Exhibit (SOUTHEASTCON), Clemson House, Clemson U, Clemson, SC. **Information:** Dr J. T. Long, Gen'l Chm, E&CE Dept, Clemson U, Clemson, SC 29631. Tel: (803) 656-3376

Apr 5-8—Design Engineering Show/Amer Soc of Mechanical Engineers Conf, McCormick Place, Chicago, Ill. **Information:** Clapp & Poliak, Inc, Management, 245 Park Ave, New York, NY 10017. Tel: (212) 661-8410

Apr 7-9—IEEE Region 6 Conf on Energy for the Future, Braniff Place Hotel, Tucson, Ariz. **Information:** Institute of Electrical & Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Apr 12-14—IEEE Internat'l Conf on Acoustics, Speech, & Signal Processing, Marriott Hotel, Philadelphia, Pa. **Information:** Institute of Electrical & Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

SEMINARS

Jan 12-14 (Tokyo), **Feb 23-25** (Toronto), **Mar 1-3** (London), **Mar 8-10** (Paris), **Mar 15-17** (Munich)—Planning & Designing Distributed Data Processing Systems for SDLC and SNA. **Information:** Saroj K. Kar, Telecom Computer Technology, 599 N Mathilda Ave, Sunnyvale, CA 94086. Tel: (408) 735-9990

SHORT COURSES

Nov 25-27 (Ottawa, Ontario), **Dec 3-5** (Los Angeles)—Military Microprocessor Systems, Culver City. **Information:** Integrated Computer Systems, Inc, 4445 Overland Ave, Culver City, CA 90230. Tel: (213) 559-9265

Dec 3-5—Minicomputer Programming & Interfacing Techniques; **Dec 8-12**—Technology Trends in Communications; **Dec 15-17**—Microprogramming: Concepts, Trends, & Applications; **Dec 15-17**—Introduction to Nonlinear Programming; **Dec 15-19**—Satellite Communications Systems; **Jan 27-29**—Standards & Specifications, George Washington U. **Information:** Dir, Continuing Eng Educ, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

Dec 5—Computer Networks, United Engineering Ctr, New York City; **Dec 6**—Introduction to Microprocessors, Holiday Inn, Pittsburgh, Pa. **Information:** IEEE Educational Registrar, 445 Hoes Lane, Piscataway, NJ 08854. Tel: (201) 981-0060, X178

Dec 7-12—Digital Electronics for Automation & Instrumentation, Donaldson Brown Cont Educ Ctr, Virginia Polytechnic Institute and State U, Blacksburg. **Information:** Education Dept, American Chemical Society, 1155 16th St, NW, Washington, DC 20036. Tel: (202) 872-4507

Feb 23—Unique Aspects of Microcomputer Applications (tutorial), (immediately preceding COMPCON 76 Spring), Jack Tar Hotel, San Francisco. **Information:** Dr Sidney Fernbach, Computer Dept L-61, Lawrence Livermore Laboratory, PO Box 808, Livermore, CA 94550

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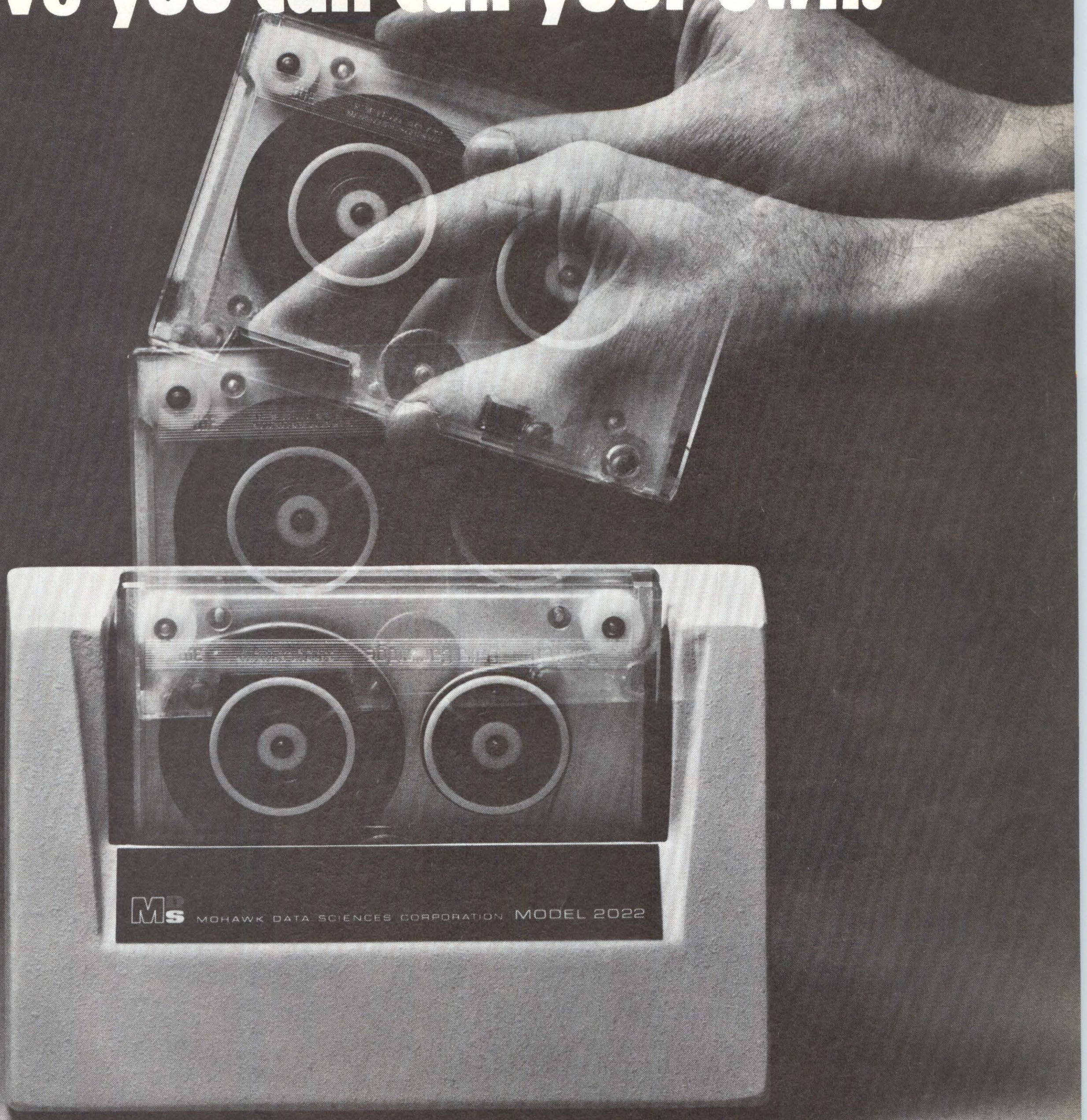

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Performance features include: 30-ips read or write, 90-ips search and rewind, read-after-write check, 250 to 1600 bpi, phase or bi-phase encoding on 1, 2, or 4 tracks, and total capacity of 23 million bits.

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INTRODUCING THE EC SERIES –A NEW LINE OF

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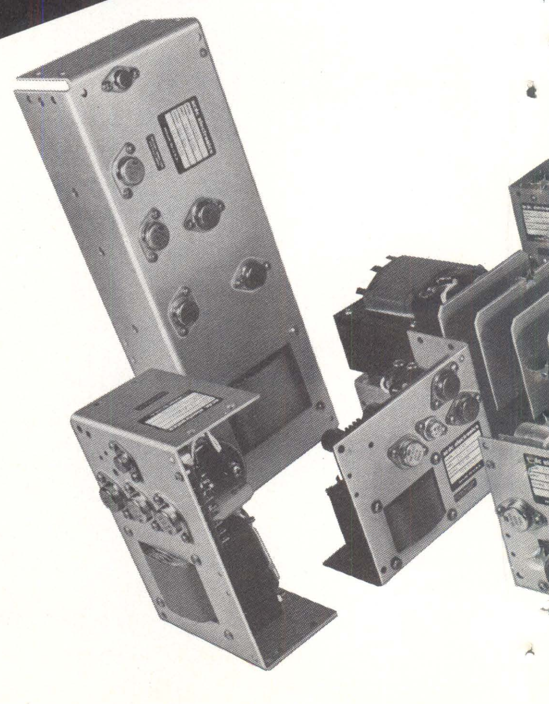

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SINGLE OUTPUT POWER SUPPLIES

Nominal Output Voltage	Max. Current (amps)	Model Number	Price 1	Price 100	Price 250
2 V.	3.0	EC2N3	$ 31.00	$ 24.95	$ 22.95
	6.0	EC2N6	51.00	41.50	39.00
	9.5	EC2N9.5	63.00	51.00	48.50
	12.0	EC2N12	80.00	65.50	62.00
	17.0	EC2N17	101.00	82.00	78.00
	25.0	EC2N25	137.00	112.00	106.00
5 V.	3.0	EC5N3	31.00	24.95	22.95
	6.0	EC5N6	51.00	41.50	39.00
	9.5	EC5N9.5	63.00	51.00	48.50
	12.0	EC5N12	80.00	65.50	62.00
	17.0	EC5N17	101.00	82.00	78.00
	25.0	EC5N25	137.00	112.00	106.00
6 V.	2.6	EC6N2.6	31.00	24.95	22.95
	5.4	EC6N5.4	51.00	41.50	39.00
	8.5	EC6N8.5	63.00	51.00	48.50
	11.0	EC6N11	80.00	65.50	62.00
	15.0	EC6N15	101.00	82.00	78.00
	23.0	EC6N23	137.00	112.00	106.00
12 V.	2.2	EC12N2.2	31.00	24.95	22.95
	3.5	EC12N3.5	51.00	41.50	39.00
	6.0	EC12N6	63.00	51.00	48.50
	7.5	EC12N7.5	80.00	65.50	62.00
	11.0	EC12N10	101.00	82.00	78.00
	16.0	EC12N16	137.00	112.00	106.00
15 V.	1.8	EC15N1.8	31.00	24.95	22.95
	3.0	EC15N3	51.00	41.50	39.00
	5.0	EC15N5	63.00	51.00	48.50
	6.5	EC15N6.5	80.00	65.50	62.00
	9.5	EC15N9.5	101.00	82.00	78.00
	14.0	EC15N14	137.00	112.00	106.00
20 V.	1.5	EC20N1.5	31.00	24.95	22.95
	2.5	EC20N2.5	51.00	41.50	39.00
	4.2	EC20N4.2	63.00	51.00	48.50
	5.3	EC20N5.3	80.00	65.50	62.00
	8.0	EC20N8	101.00	82.00	78.00
	11.0	EC20N11	137.00	112.00	106.00
24 V.	1.3	EC24N1.3	31.00	24.95	22.95
	2.4	EC24N2.4	51.00	41.50	39.00
	4.0	EC24N4	63.00	51.00	48.50
	5.0	EC24N5	80.00	65.50	62.00
	7.5	EC24N7.5	101.00	82.00	78.00
	10.0	EC24N10	137.00	112.00	106.00

DUAL OUTPUT POWER SUPPLIES

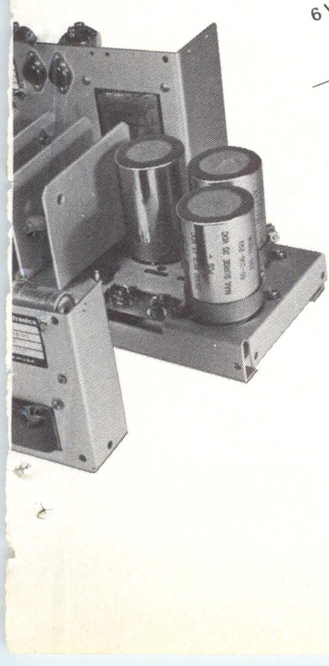
Nominal Output Voltage	Max. Current (amps)	Model Number	Price 1	Price 100	Price 250
±12/15	0.5	EC12D0.5	$ 45.00	$ 38.00	$ 35.00
±12/15	1.5	EC12D1.5	69.00	57.00	53.00
±12	3.0	EC12D3	89.00	72.00	67.00
±15	3.0	EC15D3	89.00	72.00	67.00
±12	5.0	EC12D5	122.00	99.00	92.00
±15	5.0	EC15D5	122.00	99.00	92.00

TRIPLE OUTPUT POWER SUPPLIES

Nominal Output Voltage	Max. Current (amps)	Model Number	Price 1	Price 100	Price 250
5V ±12/15	6.0 1.0	ET401	$113.00	$ 92.00	$ 85.00
5V ±12	12 3	ET601	165.00	135.00	125.00
5V ±15	12 3	ET602	165.00	135.00	125.00

OVP MODULES

Rated output current of module	Price 1	Price 100	Price 250
0 to 12 Amps	$ 8.00	$ 7.50	$ 6.50
12 to 25 Amps	12.00	10.50	10.00



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by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

System Installation Criteria

In the design and implementation of an information system, one area most likely to have not been given proper emphasis is the actual installation of the system. Considerable concern for planning and engineering is always present during the development phases. Prototypes are fabricated and extensively tested in highly controlled, sterile laboratory environments. The system design personnel then devote significant effort to establishing proper manufacturing techniques. When the question of final system installation is addressed, however, normal practice is to employ some previously defined parameters.

The cost of any device has no relationship to its importance in an information system. Though it may be stated that system importance with respect to remote devices is proportional to the sensitivity of the data to be generated or received by those devices, this is no longer applicable when considering system installation. A particular application may have a remote terminal installed at a location distant from the central processor that exchanges data with that central processor only occasionally. It may be clearly established that its information is of only minor importance to the application and, therefore, its non-availability will have minimal if any impact on the total application objective. When installation is considered, however, the relative importance of the associated data is no longer pertinent. If that insignificant remote site is incompatible with its physical installation, transient malfunctions can be generated at the remote location which can have negative and even devastating effects on the total system.

Four major areas require specialized attention when defining installation criteria: primary power, system ground, static energy, and environmental ambience; and the system designer must establish, as part of a device's installation requirement, stringent criteria for each. Not only should minimum and maximum parameter values be defined, but the installation specification should clearly establish associated testing and protection techniques. It is normal practice to define a range of voltage values within which a device is expected to operate. The same specification, however, should also identify how installation engineering personnel can test for a minimum and maximum adherence to this requirement. In addition, the specification should identify effects on performance to be expected in the event of violation of this minimum or maximum level.

These parameter values are violated occasionally, which results in the associated device exhibiting certain performance malfunction symptoms that are typically well known to the design personnel but seldom conveyed to field-maintenance or installation personnel. Usually, once the symptoms are identified, the proper source of abnormal characteristics can be easily addressed.

Primary Power

Every device that depends upon primary power has an established range of primary power values within which the device will operate. The greatest cause of malfunction in this area does not come from an absolute degradation of these levels—rather, from transient conditions occurring within the primary power source used by the device. It is recommended that every installation be provided a separate primary power source.

Installing a remote terminal by merely connecting it to a standard wall outlet in a typical office environment is a major problem source. Sharing this primary power source with other office equipment, such as typewriters or copying machines, can induce transient conditions far beyond what the terminal's power supply is able to adequately filter or regulate.

A recent example was a CRT terminal sharing a primary power circuit with an electric stapler. Whenever the stapler was activated, a 10-A surge was induced into the primary power circuit. Although the transient was of short duration, it was sufficient to couple into the CRT power supply. Under certain conditions, this transient caused errors in internal data stored in the terminal memory; at other times it caused the keyboard to assume a locked condition. Naturally, performance reports from the terminal operator and the error reports accumulated by the central processor led investigators in different directions.

System Ground

Since all data-oriented devices associated with a digital information system perform their functions in a dc environment, existence of a commonly recognized system ground is mandatory for a common signal reference. Often assumed is that the power ground circuit is a perfectly adequate system ground—until extensive "randomized" error conditions are found. A malfunctioning terminal site recently investigated showed that although a 3-prong power outlet was provided, only a 2-conductor power cable had been

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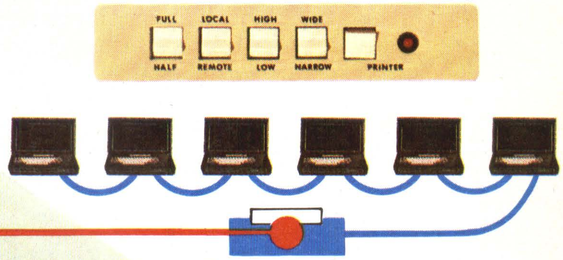

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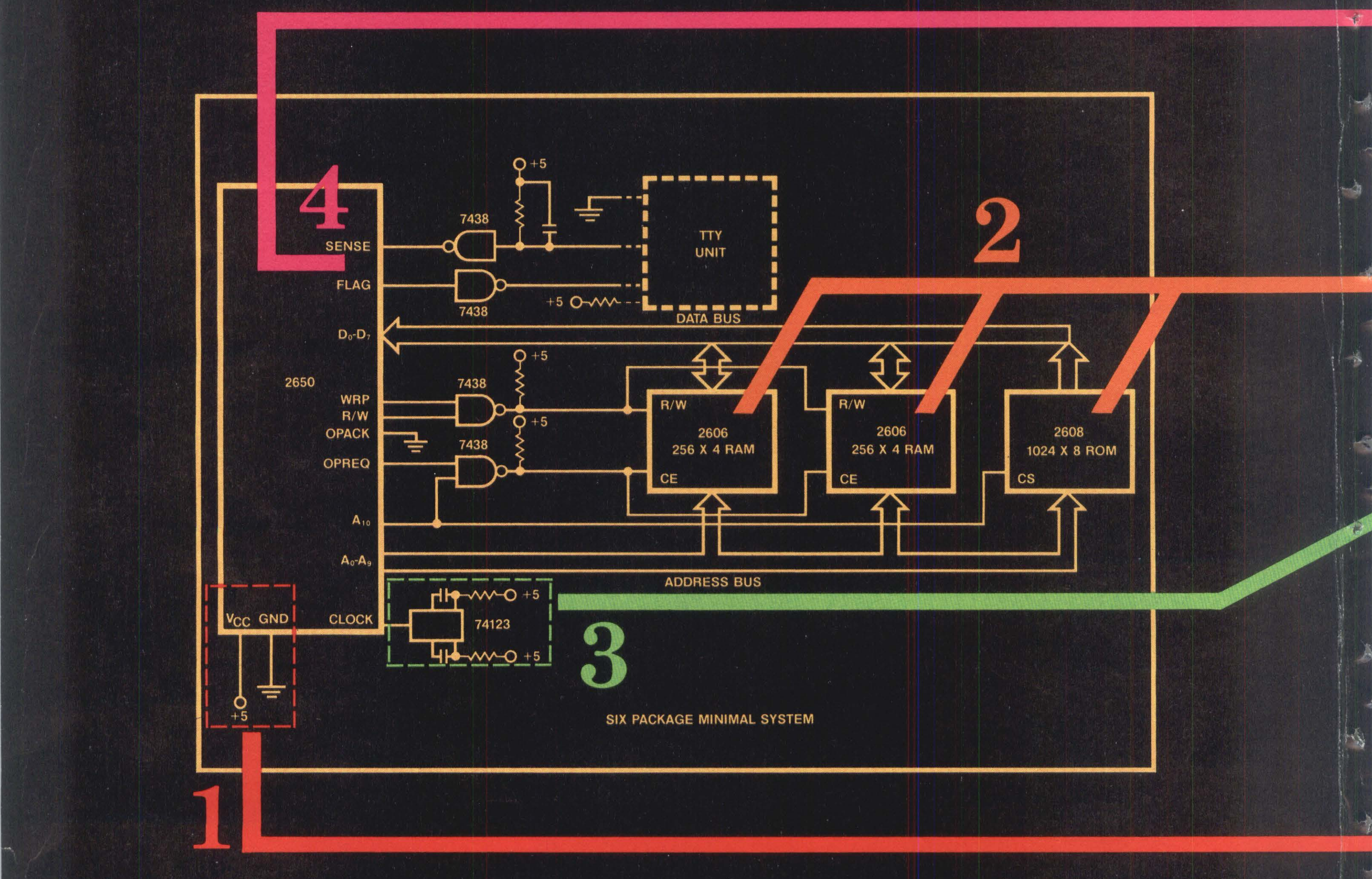

The 2650–static, 5V, TTL compatible, 8-bit μP.

Conceptual simplicity is the key to the 2650's ease of design. This μP is static, not dynamic. Its multiple addressing modes mean fewer instructions. Even the instruction set is extra powerful, to increase coding efficiency. Features that add up to less memory required, less design time. Less parts cost and assembly time. More value.

Illustrated: Parts for 6-package system. Can be purchased for under $100 in quantities of 1.

How much less than $100? In large quantities, the parts could go below $50. But what's most important is that if you build a larger system—perhaps with 5 or 10 times the memory, plus more I/O—you'll do it with the greatest of ease, and increase your savings still further. Because the 2650 won't need the special (and expensive) memory and LSI I/O chips required in other microcomputer systems. What's an outstanding value in small systems becomes an unbeatable value as the systems get larger. Convince yourself by looking at this beautifully simple Teletype system, a typical example.

1 Only one +5V power supply drives everything in the system; and this microprocessor is really low power: just 525mW max.

2 Standard, low-cost memories—your choice. This 6-package system with TTY interface uses only 3 ICs to give you 1024 bytes of standard ROM, 256 bytes of standard RAM. ROM can contain bootstrap loader and I/O driver programs for the TTY, plus operating programs for the system. Other programs plus data can also be in the ROM or written into the RAM by the TTY. Or use a PROM instead of a ROM for maximum flexibility.

3 Single-phase, TTL-compatible clock input eliminates the nest of transistors, crystal and extra ICs some other microprocessors require. Simple. Cheap. Works better.

MICROPROCESSOR.

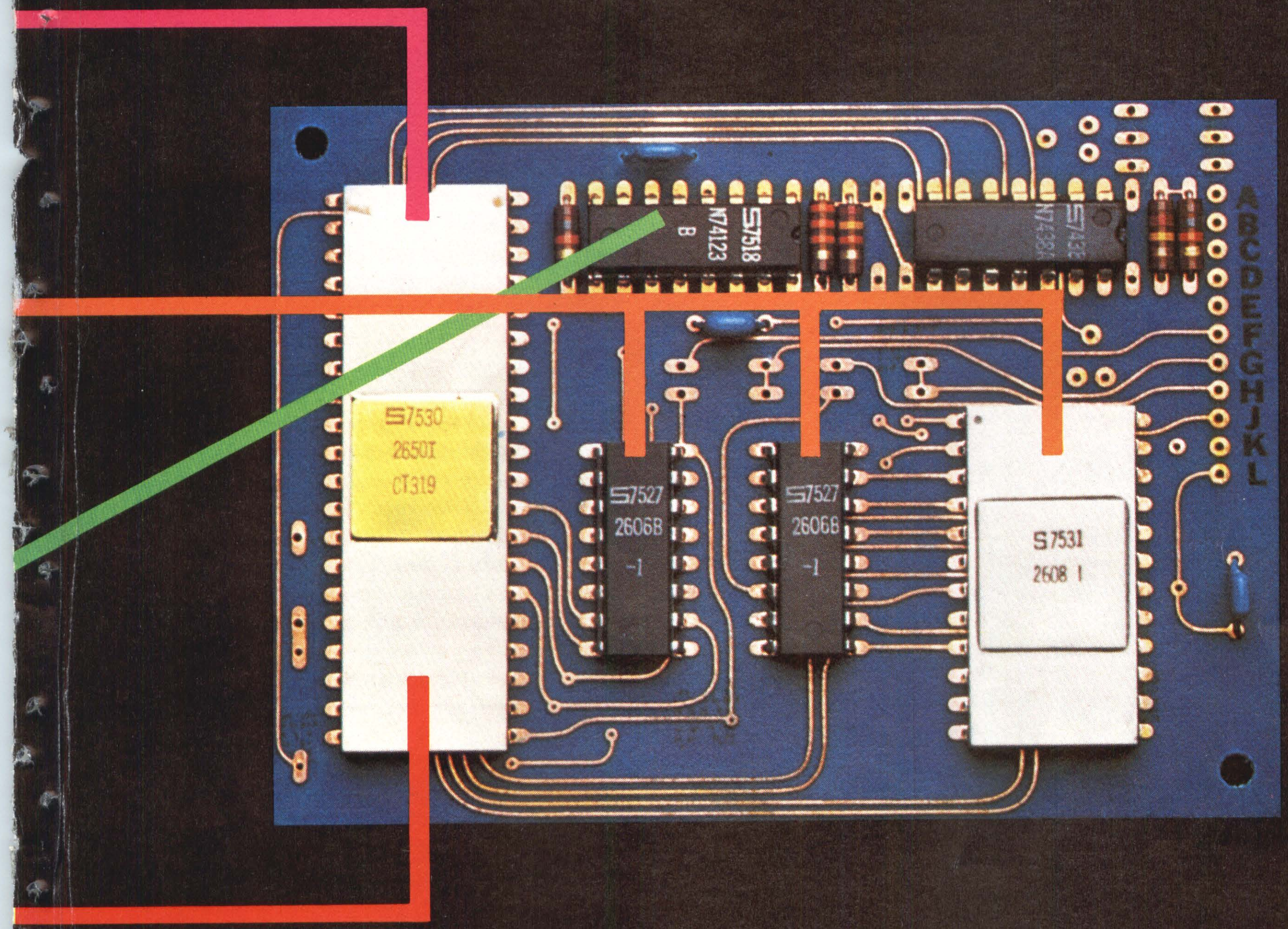

Photo approximately twice actual size.

4 On-chip serial interface eliminates a 24-pin IC. And its cost. And its space. And its connections.

5 Where are the special interface chips? There aren't any in this sample system. And not much in any other system you might design with the 2650. With much of the I/O built into the 2650, you can interface the I/O devices with simple, low-cost, industry-standard 74LS, 7400 and 8T circuits.

For instance, get both input and output with the 8T31 Bidirectional I/O Port. Or take the 8T26 Quad Bus Driver as another example. Signetics offers fifty 8T types and nearly everything in 74LS and 7400—all low cost, all industry standards. Lower parts cost means much greater value.

Software and people to back the 2650 are here now.

Cross assemblers and simulators are available in batch and on timeshare. (The assemblers come in both 32-and 16-bit formats because we realize that not every-one has a 32-bit machine.) And there's a prototyping card (CPU, RAM, ROM) with debug firmware. Documentation, manuals, application notes. Plus training seminars and on-the-spot Field Applications Engineer assistance.

You get more computer with fewer parts at less cost with the 2650. That's high-technology value. Send now for complete details and prove it to yourself.

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☐ Call me to answer questions I have.
☐ Have a Field Applications Engineer make an appointment with me soon.

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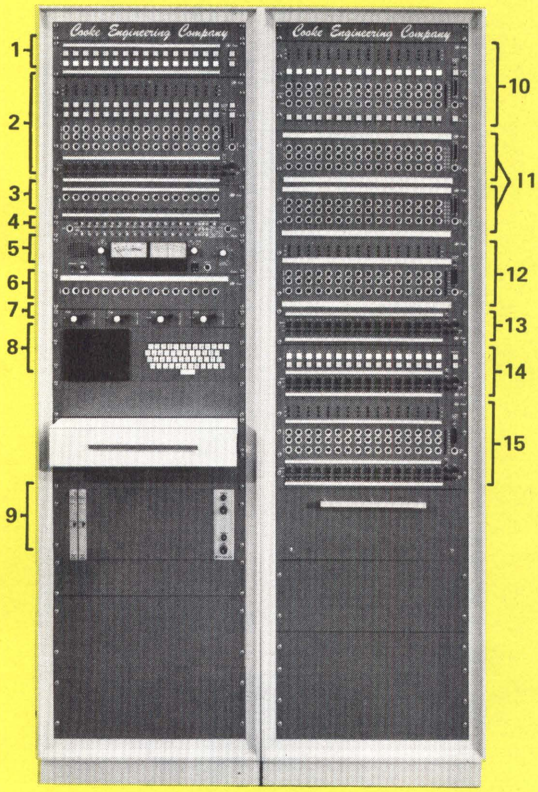
CIRCLE 13 ON INQUIRY CARD

TECH CONTROL



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8. Typical video display terminal
9. Typical Modems
10. Programmable digital switching with individual channel monitoring
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used to connect that outlet to the primary power source in the building. As a result, the terminal and associated modem were in a floating environment with respect to signal ground. Lack of a proper system ground in this installation created major transient malfunctions.

Even when a ground is provided through the power outlet—depending on the routing of the power cable within the building—it is quite possible that a potential between terminal location and true ground can exist. For example, the telephone companies' installations of communications lines typically establish their own true ground reference. With the digital equipment grounded to the power ground, a potential between the telephone company ground and digital equipment ground can exist. The result is ground loop current, which permits coupling adverse transient conditions into the system. Sometimes, such an improper system configuration will operate without any obvious malfunctions. When certain environmental factors are induced, however, evidence of randomized error conditions begins to appear.

A classic grounding problem is connection of the signal ground and frame ground leads in the EIA (Electronic Industries Association) interface cable between the digital equipment and modem. The business equipment manufacturer often assumes that the signal and frame ground connections will be provided by the modem manufacturer, and, unfortunately, the modem manufacturer may have assumed the reverse. When the business equipment and modem are supplied and installed by different manufacturers and maintained by different vendors, these erroneous assumptions will exhibit themselves in the form of floating signal ground reference which, under certain conditions, may not cause any operating malfunctions. If, however, the EIA interface cable approaches its maximum 50-ft length and/or is routed through a high energy environment, such as a computer center, major problems of a momentary or transient nature can occur.

Static Energy

Many people have enjoyed surprising someone with an electric shock caused by accumulation of static electricity, such as by shuffling across a carpeted floor, which results in

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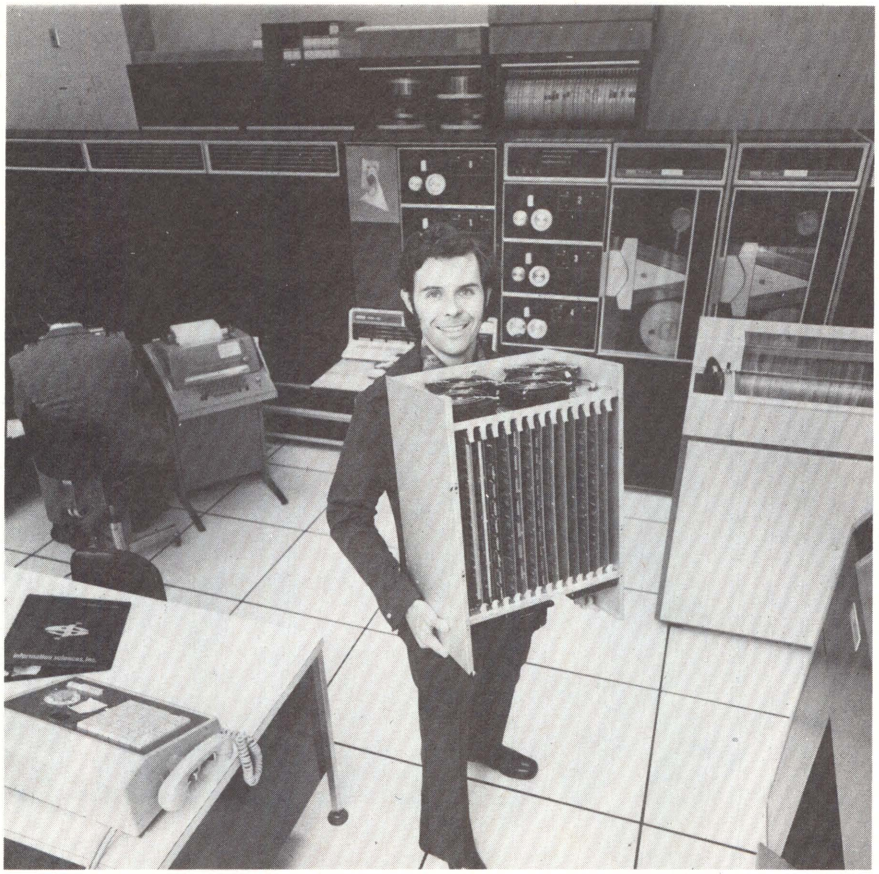

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CIRCLE 15 ON INQUIRY CARD

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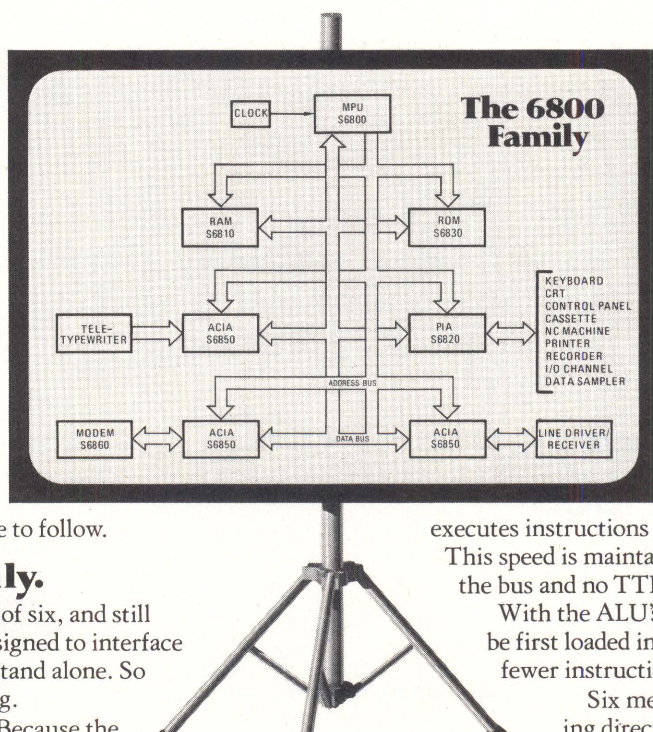
It's a whole new era for microprocessors. And a whole lot of people are sorry they started without us!

The S6800 Microprocessor family is getting rave reviews from designers, magazines and engineers—even those already committed to the 8080.

Small wonder. The powerful 8-bit N-Channel S6800 is the fastest, leanest, cheapest microprocessor system ever created.

To put it simply, it's already the industry standard that all other microprocessors will have to follow.



It's all in the family.

It's already a full-fledged family of six, and still growing. Each member was designed to interface directly with the MPU—or to stand alone. So you don't get tied up in bundling.

That can save you a bundle. Because the 6800 gives you standard LSI building blocks to put together a system without any restrictions on peripherals.

It's less costly because it requires fewer parts. It runs on just one +5V power supply instead of three. It has a more efficient instruction set, which reduces the number of locations needed in memory because of six memory addressing modes. And it needs no TTL to bring it together.

Better design gets better results.

Although the 5 volt clock operates at only 1 MHz, it still executes instructions in a minimum of 2 microseconds. This speed is maintained with up to ten devices on the bus and no TTL buffering.

With the ALU's ability to hold data, it need not be first loaded into an accumulator. The result is fewer instructions and faster program execution.

Six memory addressing modes (including direct, extended and indexed) make list processing, and the use of external memory as working registers, very fast and efficient.

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"...the most sophisticated of these new single-chip devices."

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Meet the rest of the family.

The other five that make the 6800 function so smoothly include:

The S6810 static RAM, handily organized to 128 X 8, with access time of 575 ns.

The S6820 Peripheral Interface Adapter provides two programmable 8-bit I/O channels, with full interrupt control. Each data line can be programmed to be either an input or an output. The PIA is totally bus compatible with the MPU.

The S6830 static ROM, with its 1024 x 8 organization, is the densest, fastest (575 ns access max.) read/only memory with a single power supply.

The S6850 Asynchronous Communications Interface Adapter provides data formatting and control to interface serial asynchronous communications to bus organized systems like our MPU.

The S6860 MODEM supplies modulation, demodulation and supervisory control functions for data rates up to 600 bps, using frequency shift keying.

The S6800 MPU gives you these features:

- 8-bit parallel processing
- Decimal and binary arithmetic
- Two accumulators
- 65K bytes memory addressing
- Maskable and non-maskable interrupts
- External variable length stack
- 72 basic instructions
- Six addressing modes
- Variable length instructions
- TTL compatibility
- Three state outputs
- 40-pin package
- 1MHz clock
- Single +5 volt power

The S6800 is not only the most cost-effective microprocessor system, it's also the only one that's second sourced. Motorola developed it, and we'll produce it in the kind of quantities a product this good demands.

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discharge of an electric energy impulse. This phenomenon, which measures approximately 6 to 12 kV, is a major problem in a digital equipment environment. Fortunately, however, the impulse duration is extremely short and hence of relatively low energy content. With low level digital circuits, the existence of such static energy can have detrimental consequences to the operation of the associated information system.

The typical installation of a remote terminal in an office environment permits a greater occurrence of problems resulting from static energy. One highly popular teletypewriter terminal can easily be made to suspend data transmission activity through the mere discharge of a static energy impulse to its cabinet; more than one operator of this terminal has complained about the resulting random malfunctions. Regardless of the aesthetics of the surroundings, it should be standard practice not to install these terminals in a totally carpeted environment.

One common method of eliminating difficulties from static energy is to install the device's electronics in a metallic casework which is then tied to the reference ground. This connection, however, is accomplished with a ground lead usually in the signal cable. It has been found that when a static discharge occurs, the casework conducts the resulting energy flow. This energy must then reach the reference ground through the ground lead. Since the ground lead is contained in the same cable as are the other signal leads, the adverse coupling effect still occurs.

Environmental Ambience

Every device has a range of temperature and humidity within which it will properly operate, deviation from which can result in only marginal performance or, in certain circumstances, permanent damage to the circuitry. These factors are also extremely important with respect to the media used. The paper used in a printer, the punched cards used by a card reader or punch, or the magnetic tape or cassette all exhibit a range of tolerance to these factors. The system designer must not only test and specify temperature and humidity ranges for the devices themselves but, in order to fully define the environmental specification, ranges for the associated media. Punched cards that have been stored in a high humidity environment can exhibit a wide spectrum of performance when introduced to a card reader or punch operating within its proper range.

Temperature and humidity factors must be considered not only with respect to a device's operating state but also to its storage or dormant state. A terminal that is allowed to remain inactive without primary power in a cold environment may exhibit unusual start-up characteristics. A typical example is a teletypewriter terminal which was operating during usual business days without difficulty, except for Monday mornings during the winter months. Until 10:30 am, a great number of problems and errors were occurring; from then on, however, its operation went smoothly. Investigation revealed that in an effort to conserve energy, the company was significantly reducing the heat in the office during the weekends. On a typical Sunday, the office temperature was recorded at 50 deg. It was increased early Monday morning so as to be at an acceptable level when the personnel arrived for work. Unfortunately, the terminal could not adapt to the temperature rise as quickly. Although no damage was incurred by the terminal, it was found to require almost two hours of power-on before warming to a level that permitted reliable operation. The solution was to either keep the office temperature at a higher level during the weekends or cover the terminal with an electric blanket.

Most of these factors may appear to be self-evident. Many devices, however, are completed in their design phase and moved to a location installation before the impact of these factors begins to surface. It is important that system design personnel avoid a myopic view of their equipment and its purpose and consider the realities of its installation environment. At large, centralized computer facilities, such factors are typically addressed in the manner relative to their importance. Often, however, when low cost devices for remote locations are designed, the awareness that is so integral to larger installations becomes either minimized or totally overlooked in the finalization of a product and its associated system integration. □

Instant breadboarding

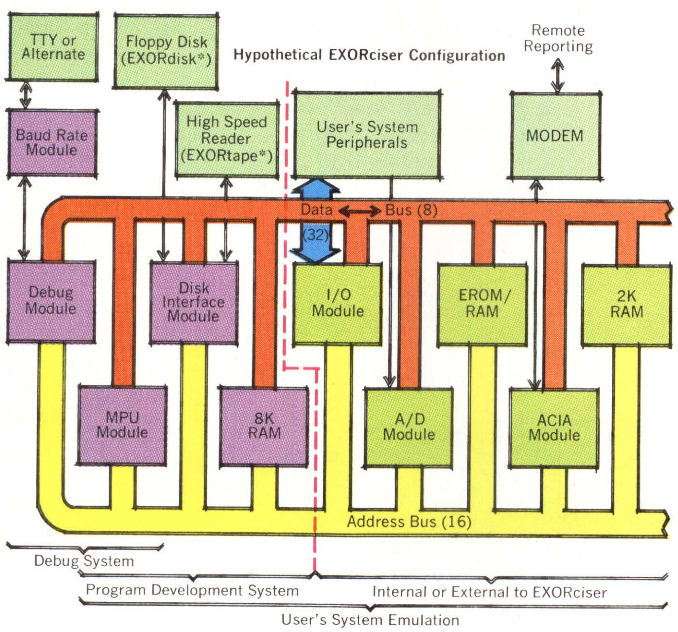
Takes the tedium from microcomputer systems design

"Donkey Work" in microcomputer systems development seems endless. It doesn't have to be! With Motorola's M6800 Family and an EXORciser*, that wasteful tedium is no longer necessary.

EXORciser configuration as a prototype of a unique M6800 system is fast and simple using standard production board options. That's instant breadboarding. It's in the M6800 tradition of simplifying and accelerating the design job. But, instant breadboarding is only one of the key functions of this triple-threat design development tool.

The EXORciser also is used to edit and assemble source programs, and its very name is derived from the functions of debugging, exorcising, and evaluating M6800 system designs in real-time.

It's both the complete system emulation tool and the debug system, too. Two systems in one. Emulation of the user system within the EXORciser chassis is achieved with the use of optional memory and I/O modules. With an external system, connect its bus as

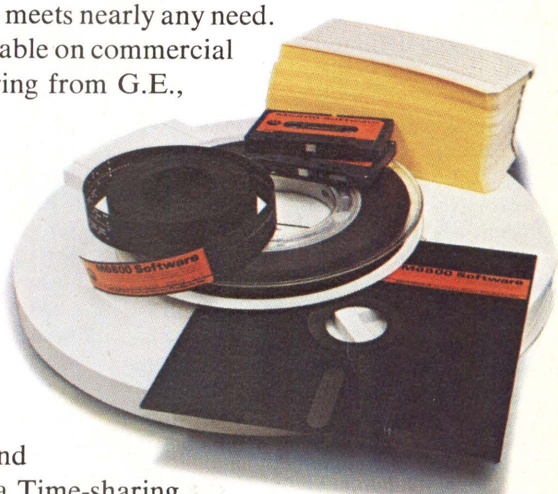


an extension of the EXORciser bus, and timeshare the EXORciser's MPU.

The basic machine consists of MPU, Debug and Baud Rate Modules, with chassis and power supply. Flexibility is enhanced by options for altering memory and I/O, the 2K Static RAM, 8K Dynamic RAM, Input/Output and ACIA modules. EXORciser options also include extender and wirewrap modules, flat ribbon interconnect cable, and battery backup.

There's a full range of M6800 support software and hardware

Support Software. M6800 software meets nearly any need. It's available on commercial timesharing from G.E.,



U.C.S. and Motorola Time-sharing. Custom and host computer software are available, and so is a full complement of M6800 Resident Software.

Evaluation Modules. Certainly the EXORciser is the ultimate M6800 system development tool, but many designers may prefer to first evaluate the operating characteristics of the various M6800 Family devices with one of several evaluation module options. These include a bare board, a completely assembled and tested module, and the same version with an 8K Dynamic RAM module plus resident software.

Support Peripherals. Other systems development tools supplement EXORciser capabilities. The EXORdisk* floppy disk unit and EXORtape* high speed tape reader are available. More items are being added.

For complete story on Motorola's M6800 support hardware and software, use the reader service number or write to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036. Any Motorola sales office or authorized Motorola distributor can handle your questions and your order.

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MOTOROLA M6800
Benchmark family for microcomputer systems.

Systems-Oriented Computers Range from 1-Board Micro to 1 Million-Word Mini

High technology, systems-oriented hardware, designed to meet needs of the systems and network computing industry, Solution Series computers—both minis and micros—provide cost-effective solutions in volume terminal-computer applications and systems capability for the supervisory and management level. The series, developed by General Automation, Inc, 1055 South West St, Anaheim, CA 92805 consists of GA-16/110, an inexpensive single-board microcomputer, designed specifically for dedicated network applications;-16/220, a 2-board microcomputer, which is claimed to offer more computing power and systems features than many currently available minicomputers; -16/330, an all-LSI minicomputer that combines 720-ns core memory with flexible packaging; and -16/440, a "maxicomputer" capable of addressing up to 1 million words of memory.

In addition to providing cost-effectiveness through advanced technology and systems architecture, simplified interfacing, and powerful instruction repertoire, the computers are both software and I/O compatible with current SPC-16 products, allowing support by field-proven operating systems and applications software and providing a choice of standard I/O drivers, peripheral controllers, and communications interfaces.

The microprogrammable, 16-bit parallel computers range in size from 1K to 1 million words of memory; both semiconductor RAM, ROM, p/ROM, and core memories are available. Units are packaged to eliminate or reduce overhead associated with chassis, console, power supply, and cabling. Optimization of minicomputers at the box level solves problems of interconnection, cooling, and power distribution, and of microcomputers at the board level allows considerable flexibility in configuring memory I/O, power supplies, enclosures, and other packaging details.

Microcomputers

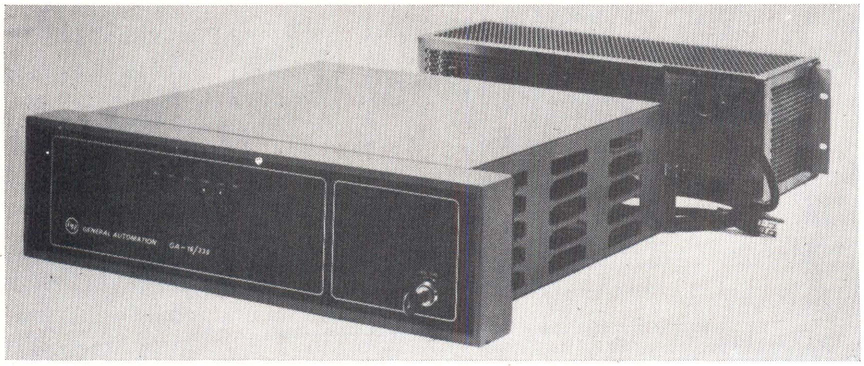
With 91 basic microprogrammed instructions, the GA-16/110 has CPU, memory, and I/O on a single, 7¾ x 11" plug-in card. CPU chips are produced using n-MOS silicon-gate process technology, contain more than 20,000 components, and attain a 450-ns microcycle time with 2-μs typ instruction execution time. The processor consists of two chips—register-arithmetic and logic unit (RALU) and control read-only memory (CROM). All calculations and logical operations occur in the RALU; CROM contains microcode that represents the instruction set, and can be expanded at a future time to augment the instruction set.

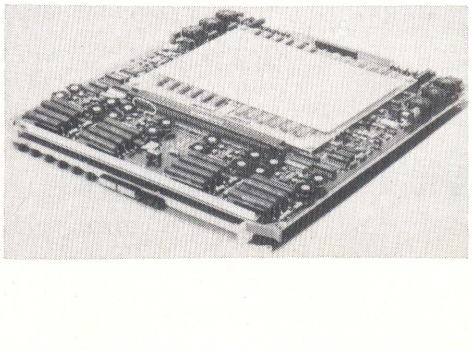
Memories include 4K and 8K 16-bit plug-in dynamic semiconductor RAM with automatic on-board refresh circuitry; piggyback ROM units, which combine 1.5K ROM with 256-words RAM, and 64 words of cold-start ROM; and 2K static RAM with 64 words of cold-start ROM, another piggyback module. Maximum memory size is 64K words in any combination.

The system incorporates integral displays and controls, asynchronous memory bus, direct addressing of 64K of memory, 11 addressing modes, and 16 general-purpose registers. Context switching, foreground/background processing, and hardware multiply/divide are provided as are power fail/auto restart, real-time clock input and interrupt, and an operations monitor alarm. Data are transferred via the fully parallel asynchronous I/O bus, under program control, or direct to/from memory via the DMA port on the memory bus.

Such options as memory parity error detection and recovery interrupt, memory write protection, and a special control store expansion module, which allows designers to add frequently used special instructions to the processor microcode, provide true flexibility and reliability.

In addition to /110 features, the 2-board /220 offers multichannel cycle-stealing DMA, integral serial I/O controller, microconsole ROM, real-time clock and full operator's controls. For special packaging, users are offered a choice of three main and auxiliary power supplies, several chassis sizes, and special ROM, p/ROM, and RAM memory configura-

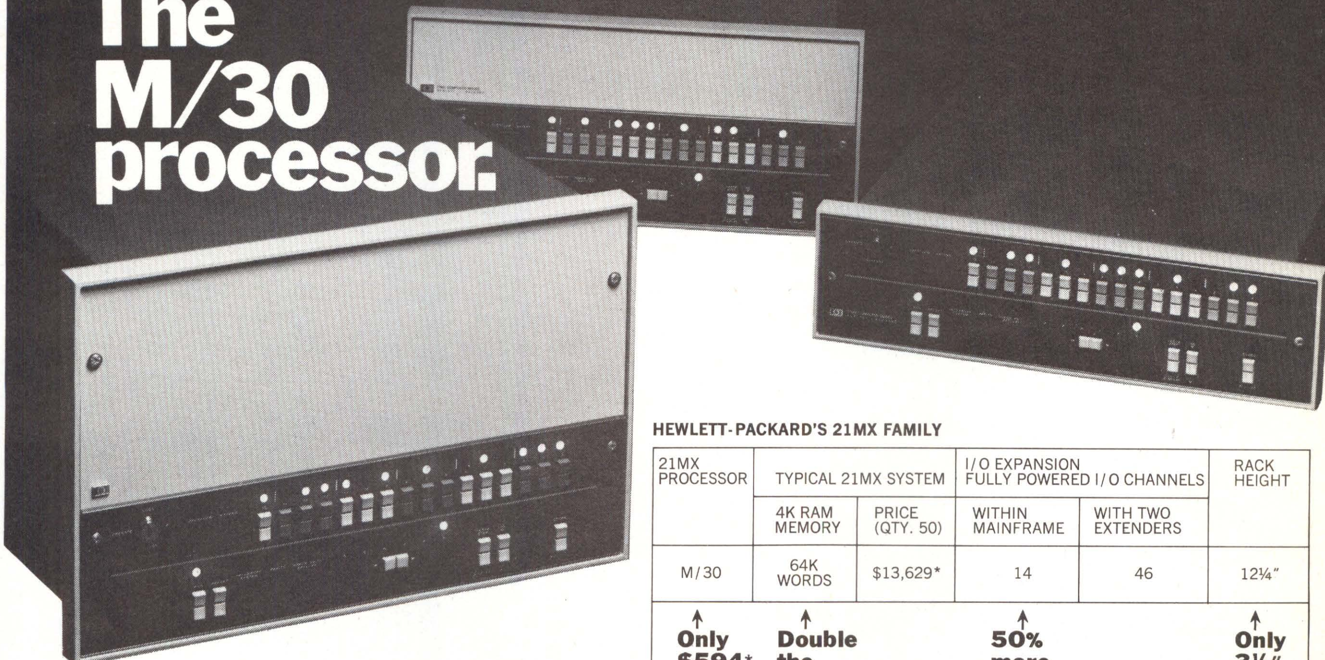




Based on a 2-chip, 16-bit LSI MOS microprocessor and 6-layer PC board packaging, General Automation's all-LSI GA-16/330 minicomputer operates with a 450-ns micro cycle time. To achieve high cost-effectiveness, the unit is available board-only or with chassis, power supply, console, or cabling

Now, a Hewlett-Packard 21MX for OEM's who think big.

The M/30 processor.



HEWLETT-PACKARD'S 21MX FAMILY

21MX PROCESSOR	TYPICAL 21MX SYSTEM		I/O EXPANSION FULLY POWERED I/O CHANNELS		RACK HEIGHT
	4K RAM MEMORY	PRICE (QTY. 50)	WITHIN MAINFRAME	WITH TWO EXTENDERS	
M/30	64K WORDS	$13,629*	14	46	12¼″
↑ **Only $594* more**	↑ **Double the memory**		↑ **50% more I/O slots**		↑ **Only 3½″ more rack space**
M/20	32K WORDS	$ 7,788*	9	41	8¾″
M/10	16K WORDS	$ 5,049*	4	36	5¼″

***Domestic USA OEM prices quantity 50.**

Now Hewlett-Packard brings 4K RAM semiconductor technology to OEM's with large memory needs. Compatible with all previous 21MX minicomputers, the new M/30 offers the same modularity, the same flexible user microprogrammability.

Not only does 4K RAM technology bring you more reliability, you also benefit from our recent February 30% price reduction on memories. (Send for your free copy of our recent "Engineering Evaluation Report." It proves the 4K RAM based 21MX minicomputer series is 50% more reliable than our previous "core" based machines.)

And take a hard look at what HP offers you in I/O. We give you more: 14 I/O slots in the M/30. But equally important they're all fully powered with vectored interrupts.

Plus Dynamic Mapping with addressability to 1 megawords.

Choose the 21MX that fits your thinking: M/10, M/20 or M/30. Ideal solutions for OEM's from 8K to 256K.

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Interdata announces minicomputer EASYWARE.

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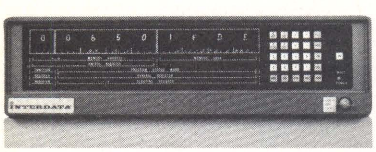

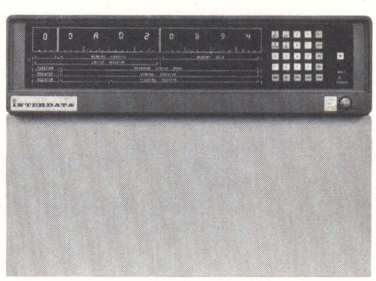

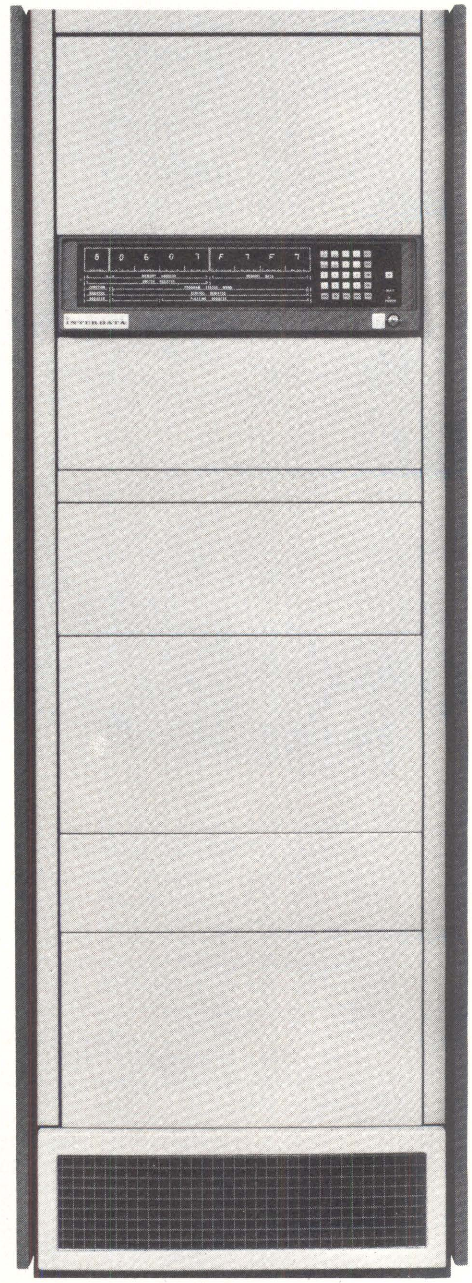

Interdata's 7/16 minicomputer is a 16-bit machine that combines high-performance with low cost. Its architecture, packaging and programmability make it a proven, cost-effective solution for the OEM buyer.

Interdata's 7/32 minicomputer is an economical 32-bit machine with a main memory expandable up to a directly-addressable million bytes of 750 ns core.

Interdata's 8/32 Megamini is the industry's most powerful 32-bit minicomputer. It is an unequalled combination of power, flexibility and reliability compactly packaged.

A family of hardware and software that's easy to work with.

Interdata offers a family of 16- and 32-bit hardware and software designed to be compatible throughout—from the low to the high end of the product line. Our Common Assembly Language enables you to go up or down in performance ranges always knowing your Interdata software will work.

Hardware.
From the beginning, Interdata built its minicomputers with a microprogrammed architecture, using the same architectural principles as the companies who build large-scale machines. As a result, our big machine architecture offers you 360/370-like instruction sets. Multiple registers. And the ability to scale-up from our 16-bit minicomputer to our one-megabyte, 32-bit Megamini.

With Interdata comes component compatibility which minimizes your inventory and guarantees interchangeability. Whether you use a 7/16, 7/32 or 8/32, you get the same front panel, power supply, memory, and same family of peripherals. Also, when you choose Interdata hardware, you can be sure anything you buy from us today is compatible with what you bought from us yesterday—or will buy from us tomorrow.

Plus software.
Interdata makes operating systems for the systems builder. Not only do they take advantage of the hardware, but they optimize the use of systems software and the human user. In addition, both the 16-bit OS and the 32-bit OS are completely compatible at all user interfaces—namely, file structure, supervisor calls, operator commands, etc.

To help the user build his system, Interdata offers a variety of higher level languages. These include: FORTRAN V—a very well-known version of FORTRAN extended for system construction. MACRO CAL (Common Assembly Language)—a macro-assembler which guarantees application program compatibility across the family. And BASIC—a simple, easy-to-use language.

Equals EASYWARE.
Interdata's philosophy has always been to make the hardware—the least expensive part of a minicomputer system—work the hardest. Our software then provides the tools which make it easier for you, and your people, to use our systems to solve your automation problems.

That's why we call it EASYWARE.

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CIRCLE 19 ON INQUIRY CARD

tions. Three classes of interrupts (NI, stack, and I/O) are provided. Autoload ROMs are an additional option.

Minicomputers

Smallest of the two minicomputers, the /330, packaged on a single board, is claimed to be the world's first all-LSI mini. The industrial/OEM unit, for use in dedicated real-time applications, offers LSI technology, microprogrammable architecture, and core memory reliability while eliminating or reducing overhead items. Centered around a 16-bit n-channel MOS processor with optional control store expansion, it features 720-ns memory cycle time; extended instruction set; full word, bit, and byte manipulation in memory and registers; and a complete interrupt structure.

Core memories are organized as 16K x 16 bits and use an asynchronous bus. The processor incorporates 25 hardware registers, 18 programmable registers, and 16 accumulators and 6 index/accumulators. The DMA bus, expandable to multichannel operation with priority sequencing, provides a 1-MHz max transfer rate. Programmed transfers via the 16-bit parallel I/O bus occur at 120 kHz, to/from memory or one of 16 programmable registers.

Most powerful of the series, the /440—a maxicomputer or megamini class machine—is implemented with Schottky MSI technology. It includes an enhanced version of the SPC-16 instruction set with standard extensions to accommodate hardware stack operations, augment transfer capabilities, and provide full left shift. With 16K basic 720-ns memory, it can address up to 1 million words using all 11 functional addressing modes. Standard processor features include 64K words of directly programmable memory, operators console, hardware multiply/divide, foreground/background registers, and dual stack processing.

Optional memory expansion and management hardware and software allows applications residing in more than 64K of memory to be executed with the same ease and efficiency as those that are directly addressable. Memory parity and write protect features improve integrity of both hardware and software.

Program languages include extended FORTRAN, COBOL, BASIC, and Macro Assemblers. Operating systems for data processing and control applications include free-standing and specialized control packages. The /110 is offered with the Control II real-time executive; /220 and /330 add capabilities provided by the Control I disc-based operating system and Control III real-time foreground/background multiprogramming system. Control IV capability available for the /440 provides a real-time multiprogramming system with memory expansion to 1 million words and memory management. All units are supported by utility software including text editors and dynamic debugging aids.

Deliveries of the /440 have started; those of the /110 are planned to begin next month, the /220 and /330 in January. Prices, in volume at maximum discounts, are /110 with 1K memory, $531; /220 with 1K memory, $765; /330 with 4K of core memory, $1950; and /440 with 16K core, $5370.

Circle 140 on Inquiry Card

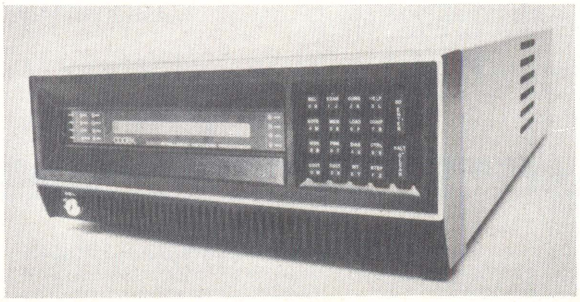
Intelligent Network Processors Optimized for Data Network Concept

Claimed to embody an architectural concept that will permit sophisticated data networks to be built without customized programming and at greatly reduced cost, Intelligent Network Processors models 6030 and 6040 have a modular, multiprocessor structure based on up-to-date microprocessor technology and are specifically optimized for the network architecture. They are intended for immediate applications in existing networks, and to facilitate growth into networks of the future.

Evolving from extensive study of user requirements and research into effective network architecture, the processors incorporate an expanded multiple-microprocessor architecture and firmware-resident internal protocol that enables them to offer a turnkey combination of cost/performance characteristics and flexibility for both point-to-point and multinode data transportation networks. They are claimed to be more intelligent than a multiplexer, and more economical and efficient than a concentrator; in addition, their network protocol is billed as being "superior to conventional packet switching." First of a family of modular communications products, the units have been introduced by Codex Corp, 15 Riverdale Ave, Newton, MA 02195 to provide low cost remote data concentration, replace conventional time-division multiplexers (TDMs), or serve as an alternative to packet switching.

Model 6030 is available in a tabletop version with processor/controller, nest to house up to 28 terminal ports, high speed network link interface, and 8 kilobytes of random-access memory. The unit is expandable to three processors, 48 kilobytes of memory, and 124 terminal port channels. Throughput ranges to 19.2 kilobits/s. Supported options include network management, data compression, performance monitoring, binary synchronous communication (BSC), asynchronous, and synchronous terminals, as well as autospeed, autoecho, operator console, and control terminal interface.

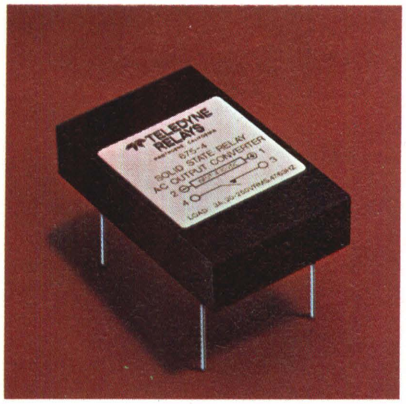
The more powerful 6040 series contains the same standard hardware but can expand to eight processors, 96 kilobytes of memory, and 252 terminal ports. Throughput ranges to 56



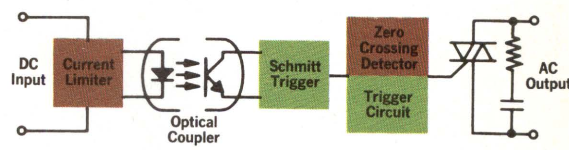
Incorporating multiple microprocessor architecture and firmware-resident internal protocol, Codex Corp's intelligent network processors provide flexibility for both point-to-point and multinode data networks. The 6030 houses up to 28 terminal ports, network link interface, and 8K of RAM, and provides throughput to 19.2 kilobits/s

Our PCB relays stack the cards in your favor.

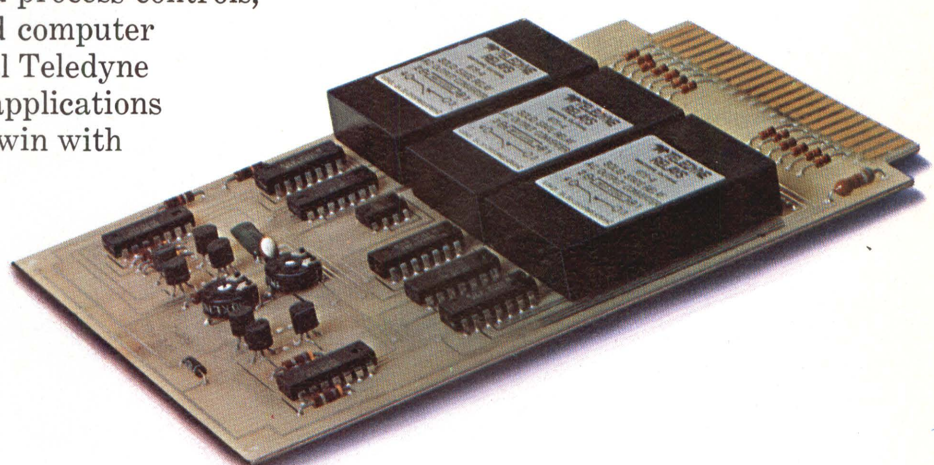
NEW



When it comes to tightly spaced pc boards, you can't lose with Teledyne's new low-profile solid state AC relays. These 0.50 in. (max.) modules are ready-made for direct pc board mounting — making them a sure bet to replace discrete circuits for close center-to-center card spacing. What's more, our low-profile AC relays are optically isolated to provide 1500V RMS isolation to protect logic lines from ac power circuits. Add to this zero voltage turn-on and a high dv/dt capability, and you're sure to beat the odds against RFI and false triggering. Designed for a maximum load of 3 amps at 250V RMS, our PCB low-profile relays come in two logic compatible input voltage ranges: 4-10V DC (model 675-4), and 10-32V DC (model 675-5). In short, they're your best choice for superior packaging and economical solid state switching circuitry for machine tool and process controls, programmable controllers and computer peripherals. Contact your local Teledyne Relays people for full data or applications help. They'll show you how to win with our PCB relays.



Functional Diagram



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CIRCLE 20 ON INQUIRY CARD

kilobits/s. In addition to 6030 options, the unit supports multinode configurations, TDM interface, automatic channel assignment, and enhanced data security.

Replacement of existing facilities by the processors is completely transparent to both computers and terminals and requires no software changes, modification of protocols, or hardware engineering by user or host-computer manufacturer. When any port of a network configuration changes, system and port characteristics can be modified on- or offline. Write-protected, nonvolatile memory contains all details on the specific configuration, such as port types, speeds, code types, routing, and similar parameters. As an option, up to four different network configurations can be stored. Each terminal port module is capable of supporting asynchronous or BSC synchronous terminals; transparent (bit serial) synchronous terminals can be interfaced. Configuration changes to port type and characteristics can be accomplished from operator console or control terminal port. No hardware strapping or board replacement is necessary.

High throughput is attained using techniques that dynamically allocate the bandwidth of the high speed network link, permitting more information to be transmitted without increasing communication line costs. Error-free operation between nodes in the network is assured by using a highly efficient full-duplex automatic repeat request scheme for node-to-node transmission.

The units are designed to support interconnection of two or more nodes in a network, allowing a variety of multinode distributed configurations —where each node may be connected to one or more neighboring nodes— to be structured. This allows processors to be located at a concentration of terminals to reduce line costs, provides alternate transmission paths for higher system availability and resource sharing, and allows intermediate nodes to serve as transfer points in loop or ring structures. Both data and control signals are passed between nodes, and end-to-end delay is less than with a conventional TDM under normal operation.

An optional network management feature provides for collection, computation, and centralized reporting of statistical measures of system performance to allow efficient utilization of communication facilities. Examples include character error rates of terminals, processor loading, memory utilization, data compression efficiency, line utilization, and traffic density. The monitoring option provides for output of reports whenever abnormal conditions or user-preset threshold levels are exceeded; the statistics option produces longer-term performance data in response to operator interrogation.

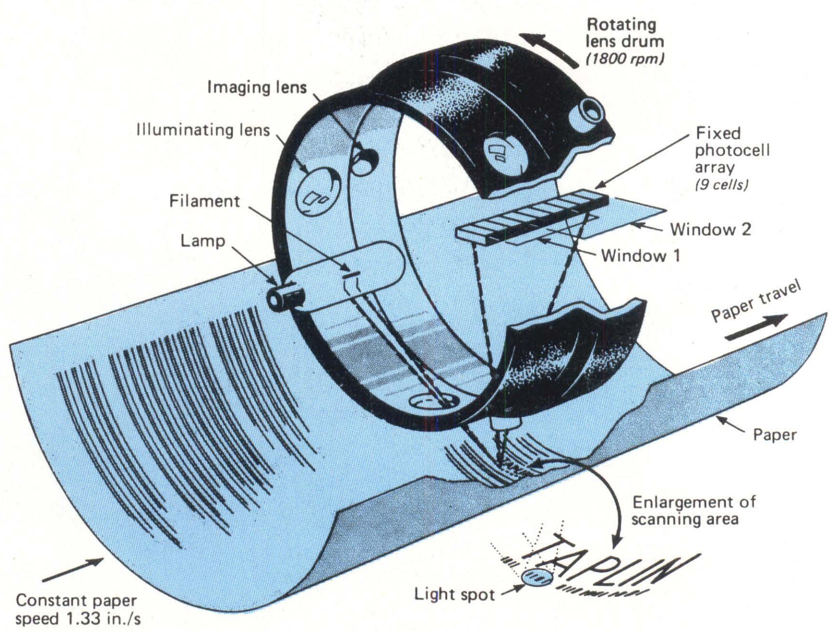
Circle 141 on Inquiry Card

High Performance OCR Reader Designed for Minicomputer Systems

Promising to make optical character recognition a logical choice for minicomputer input, the model 101 OCR page reader reads copy prepared on a typewriter using a special element that prints bar codes beneath each character. The design, developed by Taplin Business Machines, Inc, 4 Ray Ave, Burlington, MA 01803, achieves electronic and mechanical simplicity by reading only the bar codes, while the Gothic characters furnish hardcopy for future reference and serve to eliminate many data entry steps.

Key to the machine's speed and accuracy is the use of the unique barcoded typewriter font. Incorporated into the "typeball" for IBM Selectric and similar typewriters, the element prints 0.024"-high bar codes beneath the human-readable characters. The page reader ignores the letters and numerals, responding only to a complete set of four bars and three spaces. Both bars and spaces are wide (digital 1) or narrow (digital 0), establishing a 7-element arrangement of bars and spaces that define 2^7 (128) different typewriter symbols.

A single incandescent lamp serves as light source: the machine reads a line of type by scanning it with a fast rotating lens assembly that illuminates characters to be read, and focuses an image of illuminated characters onto a photocell array. The optical drum, rotating at 1800 rpm, sweeps a light beam from left to right across a line of typed characters.



Key to the reliable performance of the model 101 OCR page reader from Taplin Business Machines is the conceptually simple optical system that keeps lamp and photocells stationary and rotates the lens system instead. Arrangement of photocell elements into two viewing windows allows the machine to handle line skew and character misregistration

(*Continued on p 37*)

CIRCLE 21 ON INQUIRY CARD→

The optical drum actually houses three pairs of identical illuminating and imaging lenses, which revolve in a helical scan over the constantly traveling paper. Paper is formed into a half-cylinder by vacuum suction as it moves, permitting the optical system to view an entire line at constant focal length. Typed lines are swept with a light beam three times for each drum revolution, giving the photocell array three "looks" at each character every revolution, to permit logic circuitry to determine whether the character is recognizable or not. Using this technique, the system can operate with a reading accuracy of better than 1 char in 25,000.

Reading circuitry requires only nine photocell signal channels, since it is significantly easier to identify bar codes than to recognize closely similar Gothic characters such as O and Q. High performance is achieved by keeping lamp and photocells stationary, and rotating the lens system. The system is distinguished from earlier bar-code page readers through elimination of all incremental motion, except in the paper pick-up mechanism. All other moving parts travel or rotate at a constant rate.

Elimination of side-to-side optical scans, and line-by-line stepping of paper provides high mechanical reliability, since mechanical acceleration (involving stops, starts, direction changes, reverses), is the principal source of mechanical wear in most machines. Use of the 9-element photocell array, which spans the height of several bar codes, allows the machine to tolerate line skews of ±0.07" as well as ±0.07" vertical character misregistration.

The 101 takes approximately 10 s to read a densely-typed 8½ x 11" page, giving it a peak reading speed ceiling of 400 char/s or about 4000 words/min. Data may be read out in 8-bit parallel ASCII or other code at a burst rate of 1.56 kHz or 200 Hz, or in RS-232-C serial code at 4800 or 9600 baud. The unit incorporates an 80-char capacity storage register, which enables it to accumulate a whole line of type for subsequent readout or manipulation. In addition, it can be equipped with internal memory capability and software which will allow simple justification, editing, and other functions to be performed.

The unit measures 30" wide by 18½" deep by 37½" high, weighs 160 lb, and operates from 115- or 230-V, 50- to 60-Hz supplies. Prices are in the $10,000 or $15,000 range, and delivery is typically four weeks ARO.

Circle 142 on Inquiry Card

ECL Domination Over TTL in Computer Equipment Is Predicted

Computer logic will eventually be designed completely around emitter-coupled logic (ECL) is the prediction, which George Wells, president of Technology Marketing, Inc, 3170 Red Hill Ave, Costa Mesa, CA 92626, backs up by saying, "the ECL approach is preferred since the devices are inherently very uniform and very stable, and are excellent for driving lines. The only real reason that can be cited for not completely shifting new designs to ECL today is that most existing equipment uses other technologies, primarily transistor-transistor logic (TTL). That means you have to convert back and forth—but even that isn't much of a problem since chips to do the conversion are readily available."

However, Wells cautions, design with ECL is "a new ballgame. ECL is very fast. . . . , it can be two to three times faster than TTL, so you have to design with the higher speed in mind and follow certain layout rules."

The approach can also necessitate use of multilayer printed circuit boards, he explains. "That's certainly advantageous in terms of packaging density, and with the cost of multilayer boards coming down and the quality going up, this is much less of a penalty than in the past."

In addition, ECL requires only a 1-V swing in 3 to 4 ns, while a typical Schottky TTL requires a 5-V swing in the same time frame. Although ECL inherently generates less noise, which is a benefit; since it operates off such small voltage swings, you need to be concerned with noise levels anyway."

Prices for ECL devices using medium-scale integration are steadily declining, and major manufacturers are continually adding to the variety of ECL chips available. The user who purchases a piece of equipment using ECL rather than TTL is likely to find an improved cost/performance ratio—that is, substantially higher performance for only a slight increase in cost. With more ECL devices becoming available, and with prices coming down on the devices as well as on associated circuitry, ECL should become the dominant technology in new equipment designs.

Circle 143 on Inquiry Card

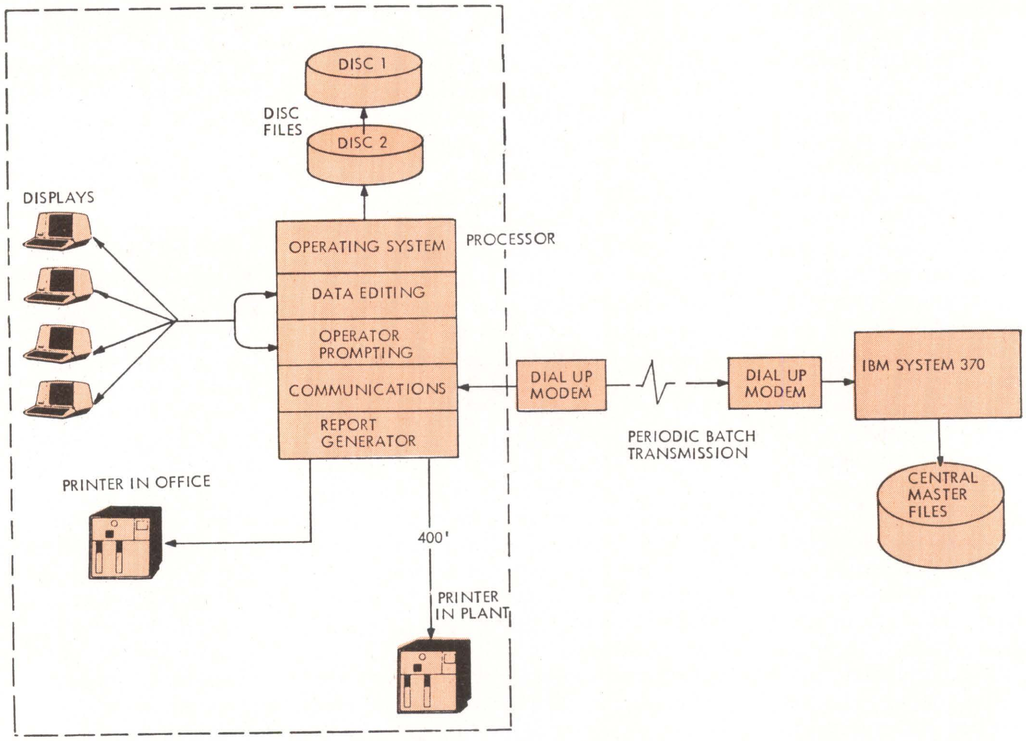
Computer System Multi-Tasks Satellite Functions for Efficiency

Giving users a single product to perform most satellite processing jobs, as well as the ability to move quickly from one processing mode to another, the low cost, PTS-1200 distributed processing system can be adapted with just a few keystrokes to perform any of the six most common processing tasks in remote offices and departments served by a distributed information network. The system combines conventional minicomputer, terminal, and peripheral hardware with a software system that integrates a package—called autoquery—of automatic data entry, editing, filing, and retrieval routines; the Macrol language for rapid applications program development; and a multitasking, multiprogramming operating system with a library of disc-resident utilities and a series of programming and debugging aids.

Basic system hardware consists of a minicomputer with a 1-μs cycle time; programmable main memory expandable up to 128 kilobytes; up to eight disc storage devices with capacity for 20 megabytes; up to 24 keyboard display terminals; and optional peripheral equipment that includes serial and line printers and a card reader.

Immediate operating capability is provided by the autoquery software package, which consists of a series of standard routines with which users can perform basic data entry, file generation, and format creation using simple keyboard commands. Ease and speed of initial start-up are amplified by the simple macro statements of the Macrol language, made up of 110 statements developed specifically for this display-oriented system. Macrol is supported by a full library of programming and debugging aids as well as a comprehensive library of utility programs. These software modules are controlled by a disc operating system which handles multi-

← CIRCLE 21 ON INQUIRY CARD



Raytheon's PTS-1200 distributed processing system contains integral disc-resident programs that perform most common satellite processing jobs. The system permits up to 24 key entry stations to share a single processor, preprocessing data to reduce CPU usage

tasking and multiprogramming without requiring the operator to perform job control activities. All system and application programs are disc resident, and all software is completely standalone. Also included in the software system are communications facilities simulating the IBM 2780 for batch transactions and emulating the IBM 3270 display terminal for online interactions.

The system, developed by Raytheon Co, Raytheon Data Systems Div, 1415 Providence Tpk, Norwood, MA 02162, is claimed to reduce communication costs for transmission between system and host computer; reduce central computer usage and size; reduce forms costs because of lower requirements for printed reports; make accurate information available on a real-time basis; increase productivity; and allow greater operator responsibility.

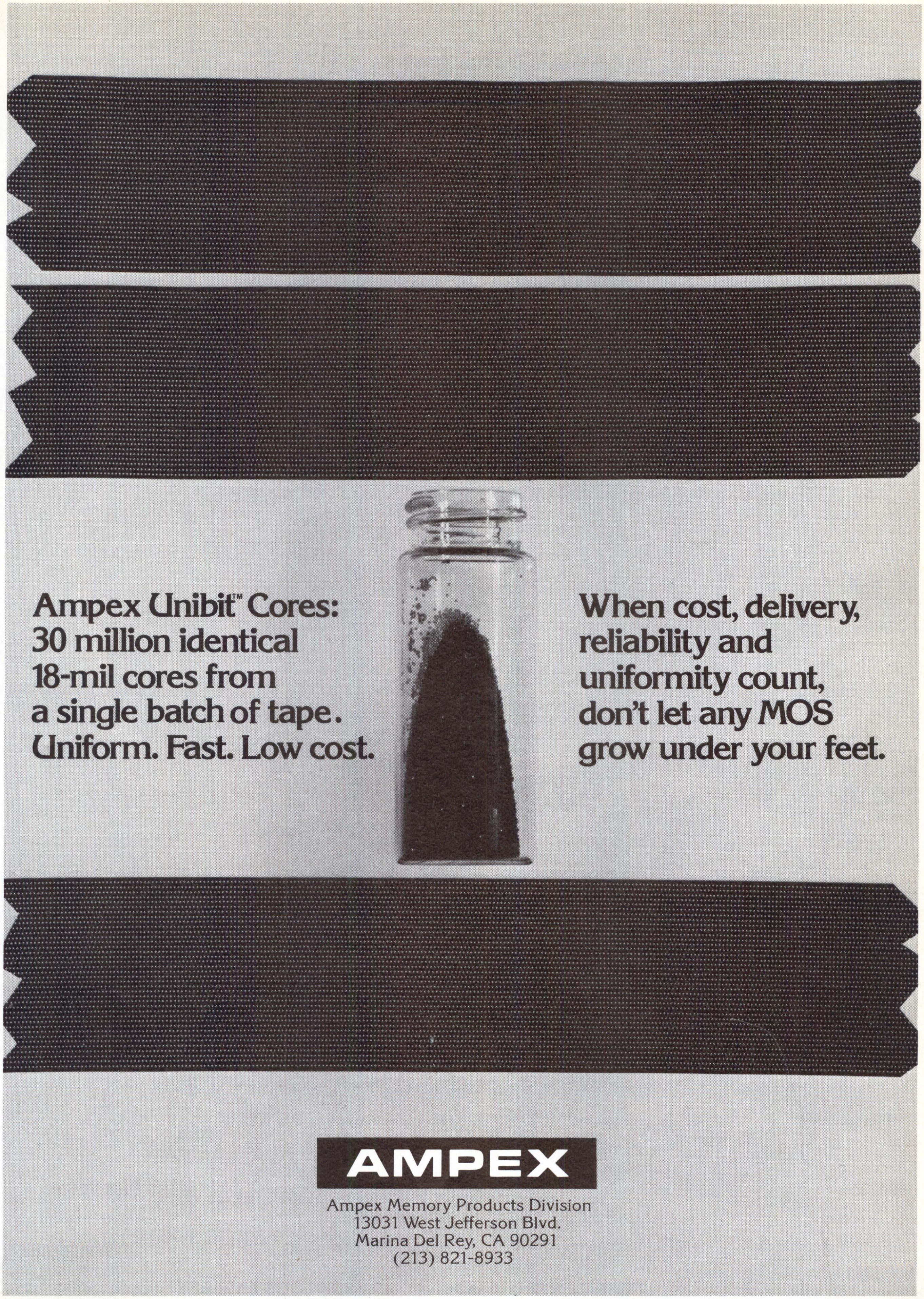
Its easy-to-use programming language will also reduce start-up costs associated with program development and maintenance. Conversion from one processing mode to another can be accomplished quickly with just a few keystrokes. In addition, the system can operate in several modes simultaneously, with more than 20 tasks occurring at the same time. Up to 24 operators with CRT/keyboard displays can share a single processor.

Prices for the system vary according to capacity, peripheral and terminal complement, and lease or purchase terms. A typical 4-station system with 1920-char displays, 64-kilobyte processor, 100-char/s serial printer, and 2.5-megabyte disc storage has a lease price of $1510/mo on a 1-yr contract, or $1264/mo on a 3-yr contract; it may be purchased for $43,100. Maintenance and software are included in the lease prices. Current deliveries are quoted at 60 days ARO.

Circle 144 on Inquiry Card

All-In-One Circuit Contains Support Devices for Scientific Calculator

An all-in-one circuit that is claimed to bring a new price/performance range to the market for scientific calculators, the MM5758, a sophisticated scientific calculator chip, operates from a 9-V battery in low cost hand-held calculators, and is suitable for many industrial applications. With the addition of only four items—display, two driver circuits, and keyboard—a powerful but inexpensive scientific calculator can be assembled around the LSI circuit, which has been introduced by Na-



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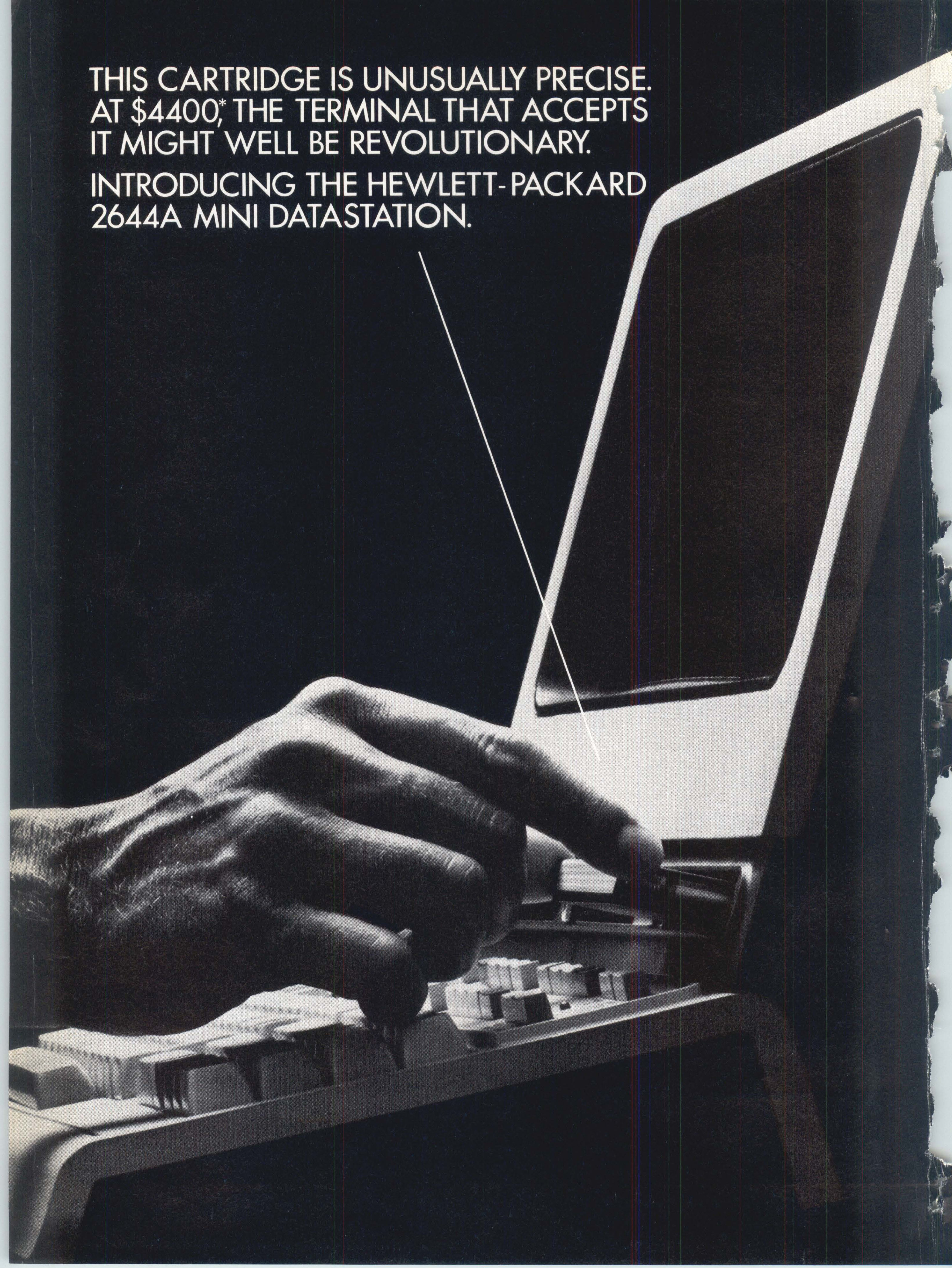
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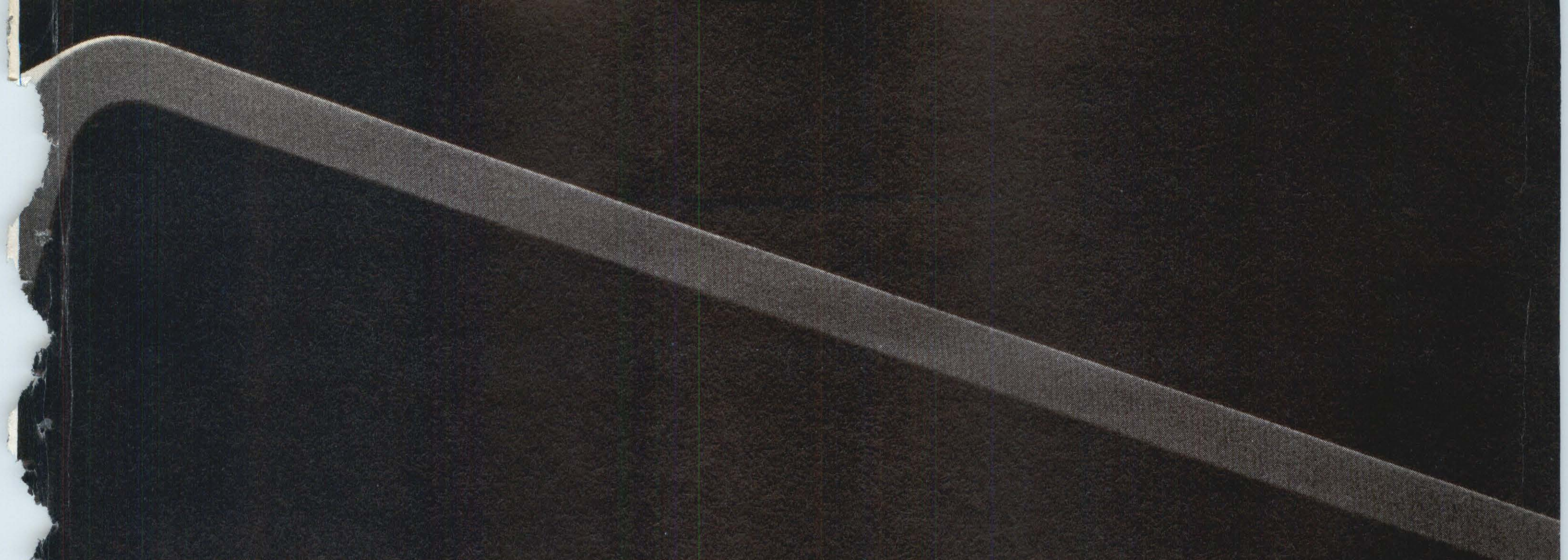
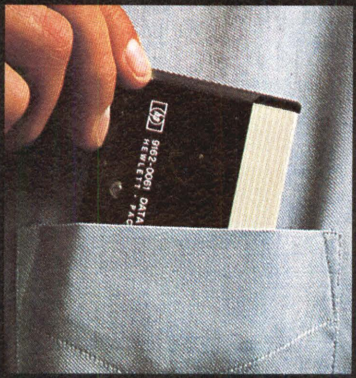


A NEW WAY TO STORE DATA CREATES A NEW KIND OF TERMINAL.



We've added twin-cartridge, integrated, local mass storage to the powerful interactive capabilities of our 2640 CRT. The result is the HP 2644A Mini DataStation, a new approach to data entry that allows many functions to be economically performed off-line that previously required costly computer time.

ENTER AND EDIT DATA OFF-LINE.

There's an enhanced 5" x 10" high-resolution display. Operator fatigue is reduced thanks to familiar-looking Roman characters delineated by a crisp 9 x 15 dot-character cell. Work proceeds efficiently with the aid of single key initiation of multiple functions, high speed search, character or block mode operation, off-screen line storage, a "protected data" switch and many other Mini DataStation convenience features.

110,000 BYTES IN EACH SHIRTPOCKET-SIZE CARTRIDGE.

That's enough for hours of typing. Precise engineering of the cartridge to HP specifications has resulted in the significantly low data loss rate of less than one byte in every 10^8. Full-width, single-track recording guarantees that this unusually high level of performance is available at every Mini DataStation, every time.

ACCURATE DATA ENTRY IS SIMPLIFIED:

By batch transmitting to the computer after data has been properly formatted and edited, efficiency is increased, errors reduced and connect costs lowered. Correct data entry is easier, thanks to the DataStation's formatting and protected field capability. A choice of four character sets lets the operator select the correct written or graphic symbol instead of an awkward approximation. And, an optional "forms" mode allows all your company forms to be pre-programmed for near instant, error-free display.

"FAIL-SAFE" ON-LINE OPERATION.

Even in the event of a computer breakdown, there is minimal work load disruption or data loss. The Mini DataStation can function independently until the computer can be brought back on line.

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Two latches provide access to every component. Want an added feature? Plug it in. Is there a new state-of-the-art option? Plug it in. Need a repair? Pop out the old. Plug in the new. There's even a built-in self-TEST key for an immediate go/no go verification by the operator.

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The HP 2644A Mini DataStation represents significant increases in throughput, data accuracy and flexibility at a price that could revolutionize your terminal operations. It is built to HP's exacting standards, and backed by HP's reputation and worldwide network of sales and service offices. For complete details, call your local HP office, or write.

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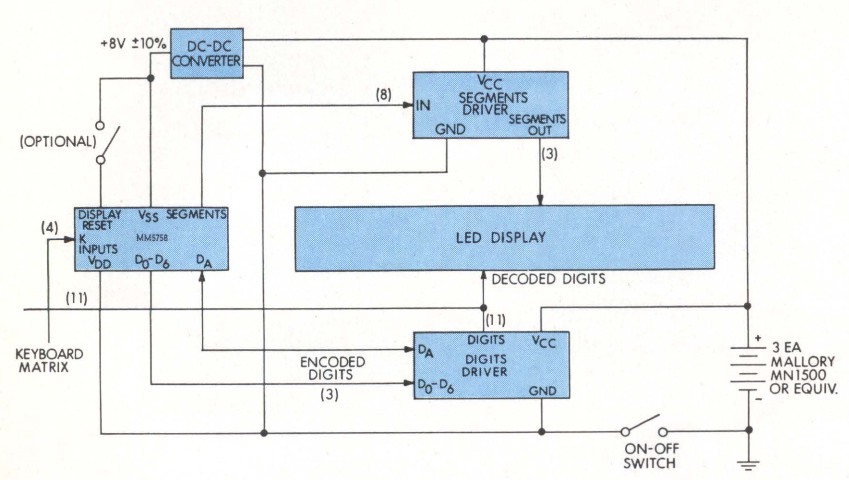
CIRCLE 22 ON INQUIRY CARD



National Semiconductor's MM5758 calculator chip incorporates support functions, allowing a powerful scientific calculator to be constructed by the addition of LED display, segments driver, and digits driver

tional Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051.

Before the MM5758 became available, a scientific calculator required several LSI circuits, segment and digit drivers for the display, keyboard debounce circuits, and power supply regulation circuits. Now, all these functions are combined in one chip that needs no support devices—not even discrete components.

The circuit permits numbers from $\pm 9.9999999 \times 10^{99}$ to $1.0000000 \times 10^{-99}$ to be entered, computed, and displayed. It also directly calculates reciprocals, square roots, exchange, and change sign. A special function displays the value of pi on demand. In addition to preprogrammed arithmetic, trigonometric, and logarithmic functions, the chip features a rollable 4-level stack that simplifies computation of problems with multinested terms, and permits review or use of intermediate solutions. Reverse Polish Notation (RPN) entry provides a logical and consistent method of keying in even complex problems. RPN logic has built-in hierarchy for increased accuracy and speed in calculating sequences involving arithmetic, trigonometric, logarithmic, power, and exponential functions.

The chip is designed to work with a 12-digit display, such as the NSA5101. It uses a mantissa of eight significant digits, two digits for the sign, and a 2-digit exponent for scientific notation. Trailing-zero suppression of the mantissa allows convenient reading of the left-justified display and conserves power. A unique battery-saver automatically shuts off the display 30 s after the last calculation without affecting register contents. The display can be restored when needed.

By adding an MM5766 programmer circuit to the calculator chip, a learn mode calculator can be created that virtually eliminates the possibility of errors in performing repetitive calculations, and saves hours of time in performing sophisticated problems. In learn mode, the programmer memorizes any combination of key entries; then in run mode, it automatically repeats them as often as desired. Up to 102 characters can be stored.

Circle 145 on Inquiry Card

Peripheral Line Expanded To Include Enhanced Printers and CRT Terminal

The Components Group of Digital Equipment Corp, One Iron Way, Marlborough, MA 01752 has added 30- and 180-char/s printers and a CRT terminal to its line of unbundled computer peripherals. All extend performance capabilities of existing series, adapting them to additional applications. Included are the LA180 DECprinter I, a low speed line printer; the LA35, a 30-char/s receive-only printer; and the VT52 video terminal.

180-Char/s Line Printer

The LA180 DECprinter I incorporates standard features that are said to make it a contender for most cost-competitive matrix printer in the industry. Its dot-matrix head has been designed for significantly quieter operation than that of many available printers, despite its high speed.

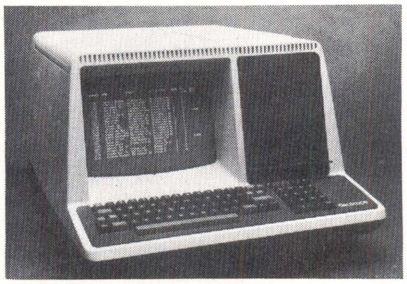
Printer design is simple and rugged. The paper feed system uses tractors with 4-pin engagement. A fine-vernier knob is provided for accurate paper positioning. A servo system transports the head along the machine's horizontal axis; carriage return has a duration of approximately 300 ms. Seven constant-current solenoid-driven wires are used to form output characters and the unit is operator-adjustable to accommodate multiple forms having up to six parts.

The LA180 forms the full 96-char ASCII character set with its 7 x 7 dot-matrix format impact head. Other features are upper and lower case symbols; ability to handle forms from 3 through 14⅞" wide; and paper-out indicator, top-of-form, self-test, and backspacing capability. Using parallel interfacing, the unit can be located up to 100 ft from the central processing unit.

Circle 146 on Inquiry Card

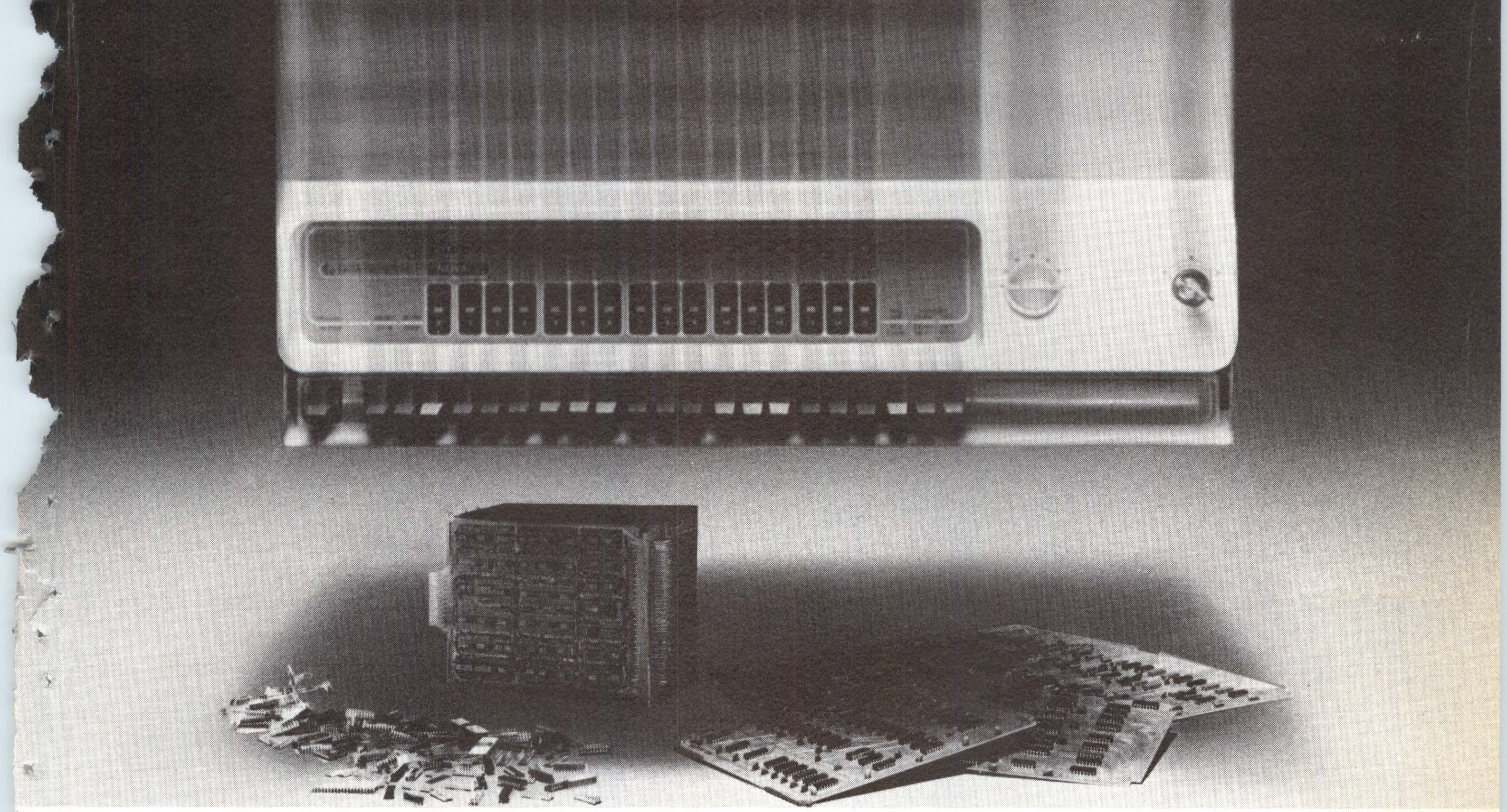
Video Terminal

Increasing performance of VT50 softcopy terminals, the VT52 video terminal has upper and lower case characters and full cursor control. Features include 24-line capacity screen, full ASCII character set, and separate numeric pad for arithmetic applications. Baud rate is adjustable from 110 to 9600. Characters are formed



By combining simple design with low density component placement, Digital Equipment Corp's VT52 video terminal assures high reliability and provides increased performance. The unit has a 24-line capacity screen and a separate numeric keypad for arithmetic applications; baud rate is adjustable from 110 to 9600

Announcing the biggest thing to ever hit the OEM market.



Here comes the biggest OEM computer you've ever seen. At some of the lowest prices you've ever seen.

The new Nova 3 from Data General.

Nova 3 has a big price edge over any competitive minicomputer. You can get a single 4K MOS Nova 3 for only $2600. (And that's before the OEM and quantity discounts get figured in.)

Nova 3 has the biggest performance of any OEM mini. It can execute instructions in 700 nanoseconds with MOS memory. And its sophisticated architecture lets you use every bit of 128K words with the optional Memory Management Unit.

And Nova 3 has the broadest range of configurations you can get in an OEM minicomputer line. There's a 4 slot Nova 3. A 12 slot Nova 3. (It has an optional expansion chassis that gives you 12 more slots of I/0.) And you can configure multiple processor Nova 3 systems.

Nova 3 also has the latest, state-of-the-art MOS memory. And the MOS chips are manufactured at our Sunnyvale, California facility. The biggest MOS RAM manufacturing capability of any minicomputer company in the world. (In fact, the only one.)

Nova 3 has the biggest array of peripherals and software. Because its hardware and software are compatible with previous Novas. The most successful 16-bit computers ever made.

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CIRCLE 23 ON INQUIRY CARD

in a 7 x 7 dot matrix. Up to 19 codes can be generated for user-assigned functions.

The convection-cooled unit operates quietly, making it suitable for low noise level environments, such as libraries and executive offices, yet it is rugged enough to stand severe environments such as machine shops, printing plants, and industrial testing stations.

Circle 147 on Inquiry Card

Receive-Only Terminal Printer

A receive-only version of the LA36 DECwriter II terminal printer, the 30-char/s LA35 printer is interfaceable to all central processing units with a 20-mA current loop or EIA RS-232-C interface. Accommodating forms from 3 to 14⅞" wide, the terminal outputs both upper and lower case characters, and prints a full 132-char width. True 30-char/s output is maintained by a "catch-up" feature that stores characters temporarily during a line feed and causes the head to print at 60 char/s until the store is depleted.

Using field-proven printhead, electronics, and mechanical components of the LA36 send/receive printer, the LA35 operates at 48 dB, making it useful in low noise level environments.

Circle 148 on Inquiry Card

Closed-Loop Approach Provides Fast, Flexible PC Design Service

Using what is claimed to be a unique operational philosophy, Diceon Electronics, Inc, 18522 Von Karman Ave, Irvine, CA 92888, has established a 20-man "closed-loop" design department. According to design chief, Marvin Cooke, "by using the closed-loop systems approach we can transform an engineering idea into a prototype or a production-run printed-circuit board on anything from the simplest configuration up to the most sophisticated multilayer high density boards."

Because interactive system equipment is used instead of more rigidly programmed data I/O type, the process lends itself to easy and fast changes, in a matter of hours, not days.

The system provides five separate checkpoints, beginning when an engineer provides a printed-circuit board schematic. The design chief first does a functional electrical check on this schematic to make sure that there have been no obvious errors between engineering and drafting; it is then given to a PCB designer who lays it out. After the design chief has rechecked it, it goes to digitizing and is checked again. The tape generated by the digitizer drives a photoplotter on both a 1-1 and a 2-1 basis. At this point, the job is checked a fourth time.

Artwork photoplotted on the 2-1 basis is retained as a master. It has an accuracy of 0.001"; when changes are needed, they are made on the 2-1 artwork which is then reduced to 1-1. Thus, final artwork has an accuracy of plus or minus 0.0005".

During any of the four checks, the originating engineer can step in and alter the design if necessary. After photoplotting, a prototype board is built, allowing the originating engineer to check the final product. Although building the prototype is an extra step, it is economically valid since problems such as proximity are impossible to anticipate, and because there may be radiation problems after a board is stuffed with components. The prototype gives the originating engineer a chance to check for such problems and to correct them before the board goes into production.

Circle 149 on Inquiry Card

Computer Company Announces Commitment to 4K Memory Chips

"It is only a matter of time before everyone in the business goes to semiconductor memory." That is the rationale given by one company representative to explain the announcement that his organization is in the process of converting to the exclusive use of 4K chips for all memory boards.

Joe Cashen, director of engineering at Prime Computer, Inc, PO Box 2600, Framingham, MA 01701, states that the present trend is to add more and more memory to systems. Because memory in the past was quite expensive, the tendency by system users was to get as much as possible out of small memories. Now, however, the relatively lower price of memory and the greater use of minicomputers and high level languages that require considerable memory have caused a demand for larger and larger memories—at prices users can afford.

The company feels that even organizations that presently mix core and semiconductor memories in large systems will eventually change to all semiconductor. Use of 4K chips permits larger memories in comparable space, with fewer packaging problems than for core.

His company is happy with the overall performance of 4K memory chips, according to Mr Cashen, and has been using 1K chips only because 4K were not available. By this fall, the company's memory boards will be totally converted to 4K. However, it will consider moving to 16K or larger chips when reliable devices of this size become available.

Circle 150 on Inquiry Card

Competitively Priced ICs Pin-to-Pin Compatible with Existing Circuits

A complete line of commercial interface circuits, designed for applications in sense amplifiers, line drivers and receivers, MOS clock drivers, peripheral drivers, core memory drivers, and high current impact printers, incorporate state-of-the-art interface technology which allows different process technologies to communicate (such as MOS/core to TTL). Pin-to-pin compatible with those supplied by other manufacturers and intended to be direct replacements for competitive devices, the circuits incorporate improved noise rejection, current/power handling capabilities, and reliability.

Among the interface circuits, introduced by ITT Semiconductors, Special Circuits, Woburn, MA 01801, are a complete series of 24 sense amps, a dual sense amp, two dual line driver/receivers, three high current printer drivers, and three high voltage gas discharge drivers. LED drivers include four dual-differential line receivers, dual-differential line driver, quad line transceiver, dual sink and source core memory driver, and quad source memory driver and quad sink memory driver. Peripheral drivers, quad TTL/MOS driver, quad TTL-CMOS 3-state, and dual TTL-MOS driver, and a sense amp/driver are also available.

Circle 151 on Inquiry Card

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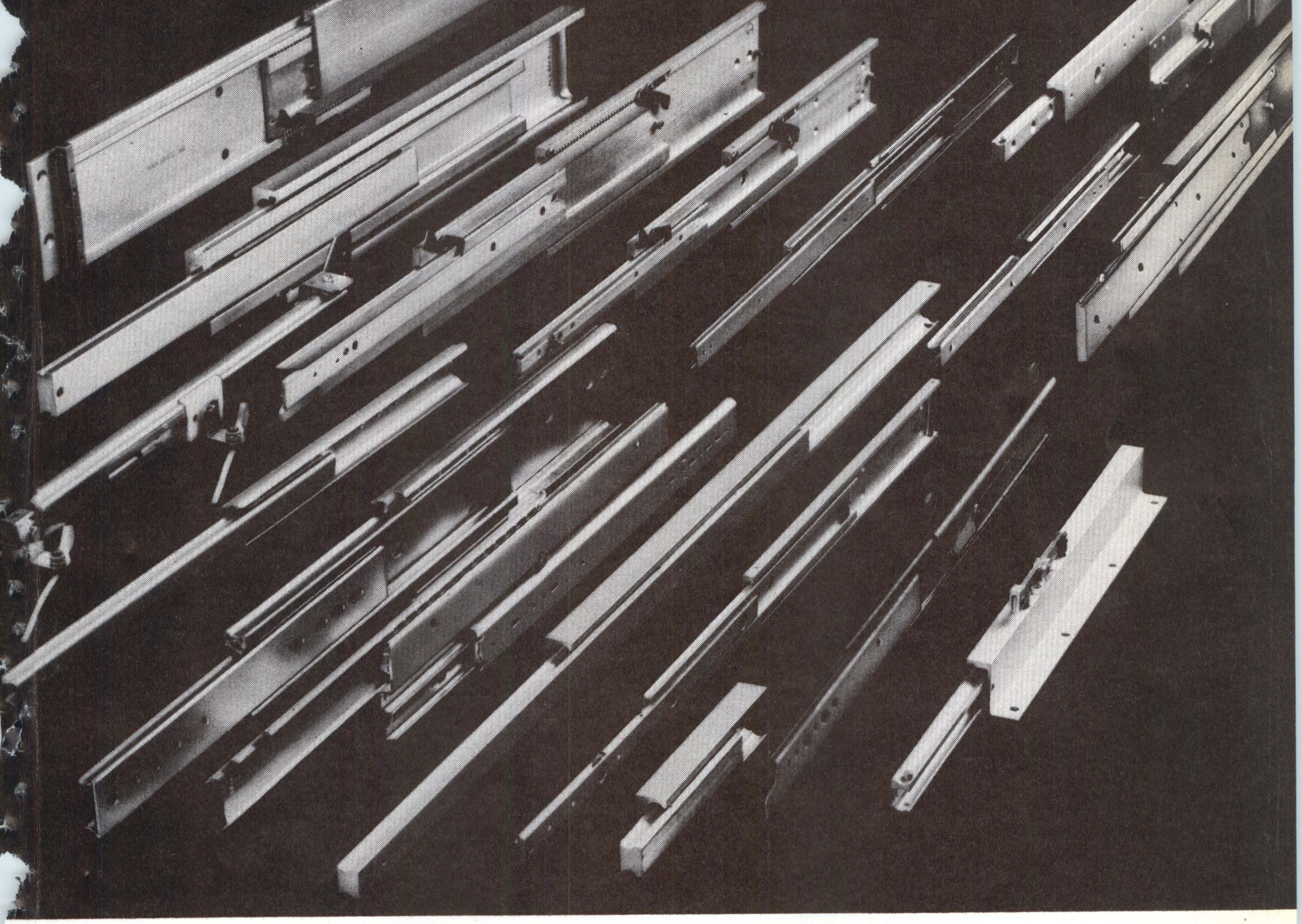

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CIRCLE 24 ON INQUIRY CARD

Add-On Memory Provides Speed Required by Sigma 500/900 Computers

ECOM[R] series H magnetic core, modular memory system, packaged in a 5¼" standalone cabinet housing up to 128 kilobytes or a 12¼" cabinet accommodating up to 512 kilobytes, is plug-compatible with and meets or exceeds all program software and technical parameters of Xerox Corp's Sigma 500 or 900 computers. Standard Memories, Inc, 2801 E Oakland Pk Blvd, Suite 307, Fort Lauderdale, FL 33306 is planning the unit specifically to meet users' needs for add-on and replacement bus-compatible memories on these computers.

Memory modules, designed for service in general systems and computer mainframe applications requiring submicrosecond random access to large banks of data, consist of core stack with associated drive, sense, and data buffer circuitry and are available in capacities of 16,384 words of 9 to 20 bits/word. Standard features include 750-ns full cycle time, 250-ns access time, and integrated circuit logic. Organization is 3D, 3-wire, with half-word byte control.

Modules may time-share or interface via the party-line interconnect technique where all address, control, and data lines are bused in parallel to all modules in the system, providing up to 20 bits/word. The interface required to service modules consists of a data register, address register, and read/write timing generator.

Optional components include memory controllers and enclosures. Packaged on 11½ x 16" PC cards, memory controller capabilities include control of 262K x 20; split read/pause/write, clear/pause/write cycle; and byte and data-save control. I/O interface is DTL/TTL compatible. Either 1-way or bidirectional busing schemes may be used. The 5¼" rack-mount enclosures, supplied with fan and power supply, house up to four 16K memory modules and two controllers; 12¼" rack-mount enclosures accommodate up to 16 memory modules and either one or two controller cards.

Circle 152 on Inquiry Card

Multifunction Data Entry System Has Remote Input Preprocessing Capability

A multifunction data entry system that preprocesses data entered from local and remote keyboard devices and optical character recognition equipment has been announced by Control Data Corp, Box O, Minneapolis, MN 55440. Accommodating from eight to 63 local and remote key entry stations operating simultaneously, CYBERDATA is a small system optimized for the data-entry function through use of comprehensive key-disc-tape software. Magnetic tapes of preprocessed information generated by the system are compatible with host systems utilizing industry-compatible tapes.

In operation, source data entered through the keyboard are formatted and edited according to pre-established procedures. Required corrections are handled immediately and validated data are temporarily stored on a cartridge disc file, having 4- or 8-million-character capacity. When a particular job is completed, data are transferred to magnetic tape for processing on the host computer. Optional communications equipment allows transmission of the data directly to the host processor.

A major operating feature is a supervisory console at the preprocessor site that allows the data entry supervisor to control, monitor, and communicate with the system at any time to check job status and workload. Two types of key-entry stations are available—the 970-32, with 32-char display capacity and the 970-480, which has a 480-char display. Both incorporate electronic 029 keyboards, which allow any rate of data input, and have video displays for checking input and for receiving error signals and instructions.

A basic system consists of processor with 56 kilobytes of memory, eight individual key stations with one controller, supervisor console, magnetic disc file, and magnetic tape unit. This configuration can be expanded to 63 local and remote data entry stations, 128 kilobytes of memory, four disc storage units, four magnetic tape units, and eight controllers.

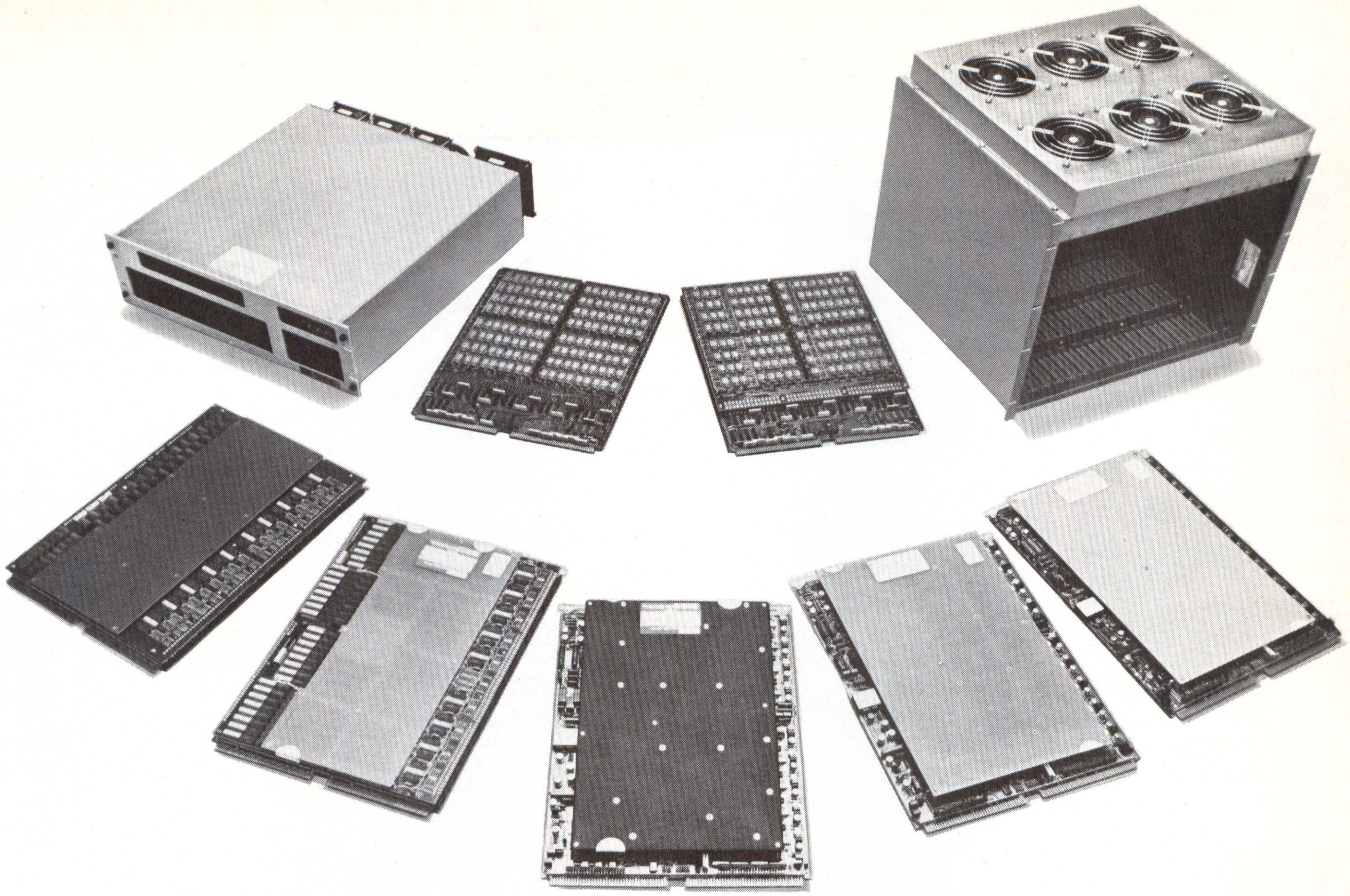
Among the optional peripherals are a 300-card/min. reader for use in media conversion and for entering format specifications and user-oriented programs. Line printers include 300- and 1200-line/min. units and feature 136-col printout and 64- and 96-char sets. The system's distributed data processing concept is broadened by use of the 929 OCR document reader and the 959 document page reader. The 929 processes original documents and single sheets or cards using a laser-beam light source. It reads at a rate of 2210 10-pitch or 1547 7-pitch char/s with a maximum throughput of 1200 documents/min. The page reader accepts typewritten, handwritten, or computer-generated source documents in the form of pages, separated fan-folds, small forms or cards, or journal tapes, scanning data at the rate of 750 char/s with a throughput of 720 full pages, or 18,000 small documents/hr.

Communication between the system and host computer is provided by a binary synchronous communications controller and software emulating IBM 3780 protocol. The controller operates at synchronous rates of up to 9600 bits/s over a 2- or 4-wire dedicated circuit, or at up to 4800 bits/s on a switched circuit.

Communication between distributed cluster remote controller or key-entry stations and the system are via full-duplex dedicated lines in a synchronous mode at 2400, 4800, or 9600 bits/s. Through use of an asynchronous controller and modems, single key-entry stations can be remoted any distance from the processor. Local supervisor and remote site operators can communicate with one another through displayed messages.

The CYBERDATA operating system (COS) provides extensive formatting, validation, and editing routines. It enables data entry supervisors to virtually duplicate main computer operation by simply selecting the edit functions appropriate to each field on a source document. All automatic features of the operating system are implemented by filling in a simple format specification sheet. Unique customer requirements are easily accommodated by adding routines through either the keyboard or card reader. Consequently, the system can be customized to meet individual customer needs. □

Circle 153 on Inquiry Card



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The beauty of it is, you can mix or match any of these in the same 5¼″ chassis, and go from 4K core to 32K NMOS cards without any basic change in the support electronics. (There's even a vertical chassis which holds up to 16 cards totalling a megabyte if you need that much.)

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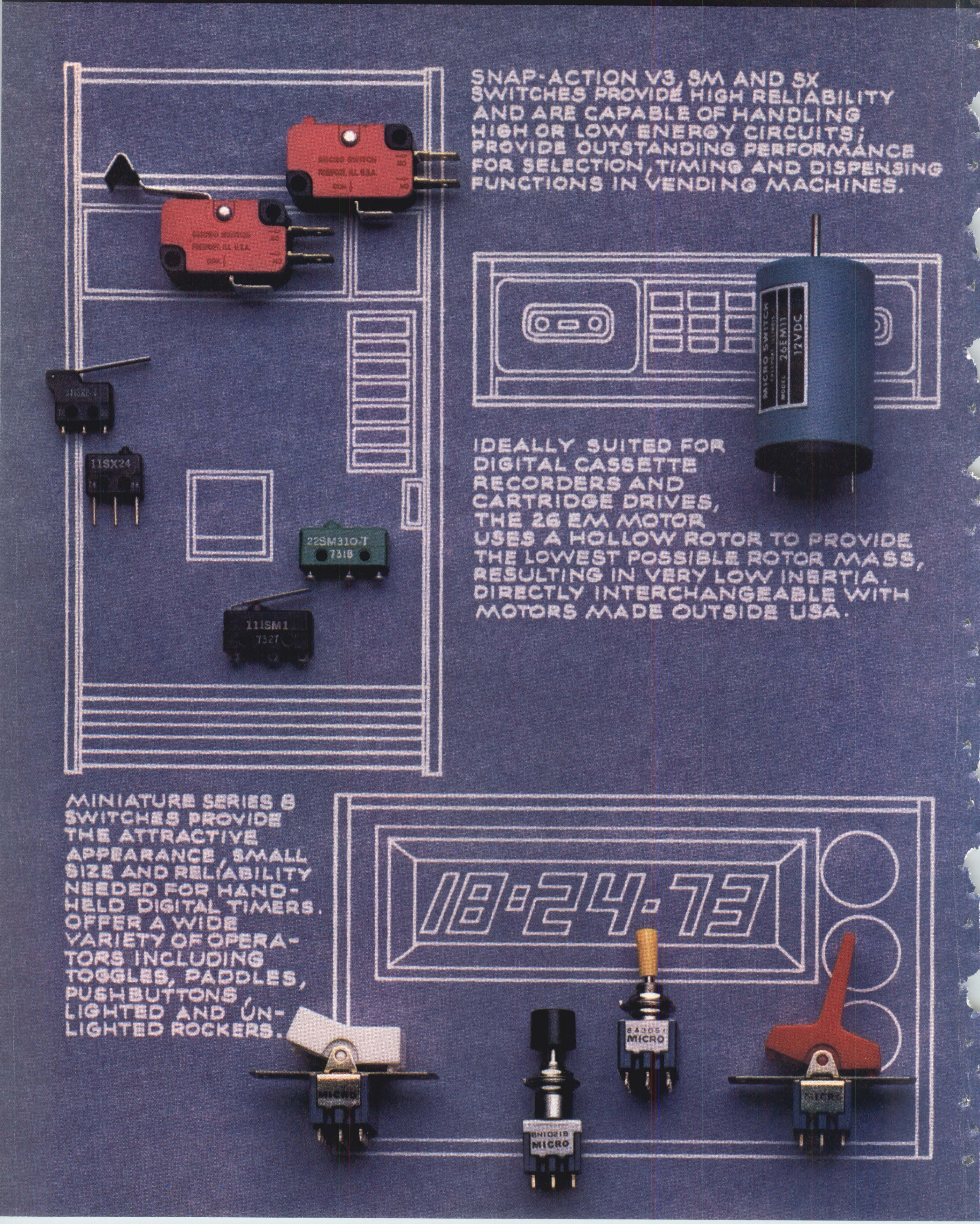
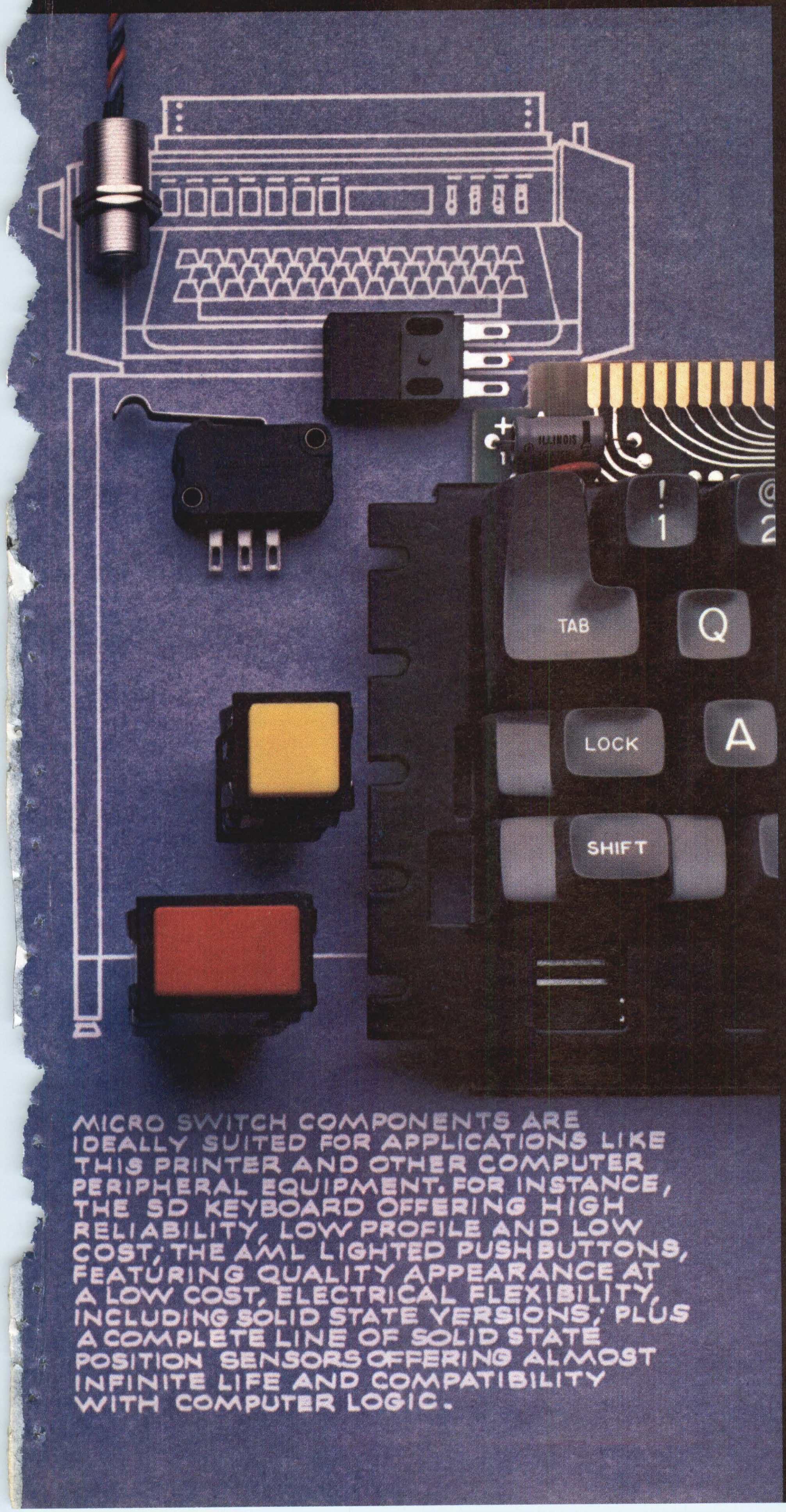
CIRCLE 25 ON INQUIRY CARD

Some of these components will probably



never wear out. The others will just come close.



The solid state keyboard, AML lighted pushbuttons and solid state position sensors you see here will probably never wear out. Because they're all solid state.

Each is based on a Hall effect integrated circuit. A circuit that's been tested through billions of operations without failing. Even once. And proven by performance in a variety of applications. The other components you see here come close. Simply because of the way they're designed and put together.

Like the long-life versions of our snap-action V3, SM and SX precision switches. Available in a wide variety of sizes, electrical capabilities and ratings, terminals, actuators, contact forms and operating characteristics—they've been tested to a mechanical life of over 10,000,000 operations.

Or the Series 8 miniature manual switches. Designed with epoxy-sealed terminals on most versions for extra reliability. And offered with virtually any operator you might need. Plus terminals that include solder, quick-connect, printed circuit or wire-wrap.

The same standards of quality and product flexibility go into the 26EM DC motor. It's a miniature motor designed with low inertia operational characteristics. And just one of a line that ranges up to the 500VM, a motor capable of accelerating to 4000 RPM and stopping over 1000 times per second.

If you'd like more information on any of these components, contact your nearest MICRO SWITCH Branch Office or Authorized Distributor.

And find out how you can get a component that goes on forever. Or at least comes very, very close.

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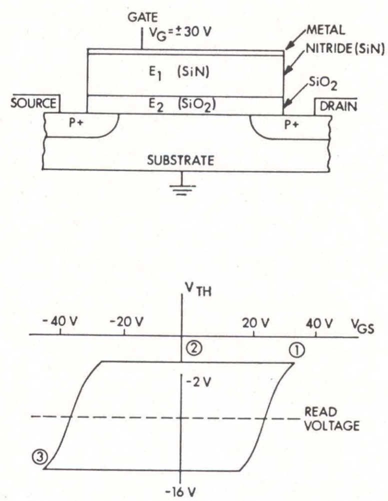
MNOS Technology Shows Promise for Military Memory Systems

A block-organized random-access memory (BORAM) system test vehicle using MNOS technology, believed to be the first memory system of this type delivered for a military application, has been accepted by the Naval Air Development Center, Warminster, Pa. Delivery by the Sperry Univac div of Sperry Rand Corp, St. Paul, Minn represents one phase of a long-term Navy development program for advanced computer hardware.

Using MNOS (metal-nitride-oxide semiconductor) transistors as basic memory cells in a large-scale integrated memory promises to overcome volatility and low radiation tolerance limitations that exist when applying conventional semiconductor memory to military systems. The MNOS single-transistor memory cell uses a variable threshold transistor (VTT) capable of storing information for long periods of time in the form of a high or low device turn-on voltage. The transistor is physically similar to an MOS transistor, with the exception of the additional silicon-oxide insulator layer (E2 of diagram) located between the silicon substrate and the silicon-nitride layer (El). Electrically, they differ in that while the MOS transistor's threshold voltage (the gate voltage at which a specified minimum drain current starts to flow) is fixed at a constant value, the VTT's threshold voltage can be set electrically to predetermined high or low values so as to represent logical "1" or "0" bits of binary information.

Mechanism of the MNOS threshold voltage change depends upon the change in the electrical charge existing near the transistor's nitride-oxide interface. For instance, the VTT threshold can be shifted to a low state by applying approximately 30 V across the gate and substrate (point 1 on hysteresis curve). This positive potential is sufficient to induce tunneling of electrons through the thin silicon oxide and into trapping states near the nitride-oxide interface. Net negative charge at this interface results in a shift of the threshold voltage to approximately –2 V (point 2) after the gate voltage is removed. The opposite effect is achieved by



Composition of MNOS transistor (top) and hysteresis curve. Technology is promising for overcoming volatility and low radiation tolerance limits for military memory systems

applying −30 V to the gate, which in turn increases the VTT threshold to approximately −16 V (point 3).

Status of the VTT can be sensed by applying a negative voltage (of a value between the two threshold extremes) to the gate and monitoring the resultant change in drain voltage. If previously set to the low threshold state, the VTT will conduct and the drain will charge to the source voltage. If previously set to the high state, no current will flow and the drain voltage will remain at its quiescent state.

The key to MNOS nonvolatile memory technology lies in the disparity of the write (charging) time, with respect to the retention (discharging) time. This is dependent mainly upon the thickness and composition of the silicon-nitride and oxide insulator layers, and the characteristics of the write voltage pulse. For instance, data retention times of up to one year are possible using 1-ms write pulses.

This nonvolatility, while providing long retention times and higher radiation resistances than those exhibited by MOS transistors, also minimizes system power dissipation, since it permits powering-down memory arrays when they are not actually performing a read or write operation. In addition, the resultant small area of silicon per memory cell permits achieving high packing densities using conservative IC layout rules. Present technology provides a density of 50,000 fully decoded bits per square inch of silicon. Since the MNOS device is generically an MOS transistor, large-scale integrated memory arrays can be incorporated on the same chip with associated high performance MOS circuits. This achieves a very high input/output performance while simultaneously reducing the array's organizational complexity.

Electron Beam Technique Offers Improved and Less Expensive IC Masks

The Electron Beam Exposure System (EBES) is said to be a major advance in the fabrication of integrated circuits (ICs). Developed at Bell Telephone Laboratories, Murray Hill, NJ, the EBES uses a beam of electrons to generate the microscopic patterns from which ICs are manufactured. Reportedly, it can produce IC master pattern masks faster, more reliably, with fewer defects, and at lower cost than masks made by existing photographic systems. The patented system has been used routinely at the Laboratories to produce master masks.

The automated, computer-controlled EBES uses an electron beam to write the intricate, microscopic IC patterns. Because electrons have a smaller equivalent wavelength than light, used in conventional mask-making processes, a much "sharper" writing beam can be generated. The EBES electron beam is focused to a spot 20 one-millionths of an inch in diameter—about one one-hundredth the width of a human hair. Even smaller spot sizes can be used, but with a corresponding increase in time and cost.

The EBES writes its intricate pattern on a chromium-coated glass substrate covered with a film of chemical "resist" which is sensitive to the electron beam. Unexposed portions of the resist and the underlying chromium are then etched out by chemicals, leaving a negative mask pattern of chromium on glass.

(Continued on p 52)

Granted, our new ADM-3 is basic. Especially if you compare it with all the smart video terminals around (our ADM-1 or -2, for example). But the $995 unit price puts it into a different perspective.

As simple as it is, the ADM-3's one-card brain can help you move a lot of data. And it's compatible with most popular computers. That means, it fits all kinds of applications. Including yours.

Here's what you get for $995. 12" diagonal screen. Full or half duplex operation at 11 selectable data rates. Bright, easy-to-read characters — 960 or 1920,* displayed in 12 or 24 rows of 80 letters. 59 data entry keys arranged like on a typewriter which keeps operator training short and basic, too. What's more, our ADM-3 is alert. It says "beep" when you come to the end of a line. The rest of the time, it just keeps cool and quiet.

Our DUMB TERMINAL also offers you room for improvements. Its RS 232C interface extension port lets you hook up hard copy printer, magnetic tape recorder or additional (smarter) data terminals. And with a few options, you can make our ADM-3 answer back. Increase its vocabulary by adding upper and lower case. Transmit and receive independently selectable rates. Even enter just numbers on a numeric key pad.

After counting all its limited blessings, you have to admit one thing: you simply couldn't ask for more for $995. At this low level, you can afford to order a dozen or more DUMB TERMINALS (and buy them at our even lower quantity discount price).

*1920 Characters is an option available at additional cost.

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INTRODUCING THE $995 DUMB TERMINAL.

Because the electron beam system can write the microscopic pattern of a single IC chip over a larger pattern area than conventional optical cameras, the mask-making process for very large chips is simplified and substantial cost savings result. The mask blank is mounted on a movable stage positioned to an accuracy of one one-millionth of an inch. The stage moves continuously while the pattern is being written, making the exposure faster and more accurate than if the stage stopped for each exposure, as with sequential optical cameras presently used in the IC industry. Circuit design instructions on magnetic tape are fed into the EBES computer, which controls both the electron beam and the movable stage, so that the mask-writing operation is entirely automatic.

Computerized Star Gazer Will Detect Unidentified Space Objects

An experimental computer-controlled surveillance system that is being developed by the Air Force System Command's Electronic Systems Div will spot "interlope" objects traveling in space. Main focus of the Ground Electro-Optical Deep Space Surveillance (GEODSS) System will be on orbiting and space-parked distant Earth satellites up to 20,000 miles from Earth. Any object traveling through the star field that does not match the relative motion of the field will be noted.

Data processing, analysis, storage, retrieval, control, and display will be handled by a Modular Computer Systems Modcomp II/45 computer. It will maintain video/analog data processing, digital interface and timing, and communications. Sensor signals will be converted from analog to digital format for the computer. These data will either be stored or cause the computer to react in an "alarm" situation. The computer will also assist in search pattern generation and will process tracking data to produce orbital elements.

MIT's Lincoln Laboratory created the prototype system and designed and installed the experimental test site. The Laboratory will also operate the test site at the White Sands Missile Test Range under Air Force contract. Testing during the next year will evaluate system components prior to setting up a fully operational version.

Satellite detection is founded on a "freeze action" technique that seemingly halts stars in their tracks. Telescope scan rate will be synchronized to the motion of the star field. Day-by-day count of all satellites and space debris circling the Earth will be maintained. Non-programmed objects that appear will be readily detected and will trigger an alarm.

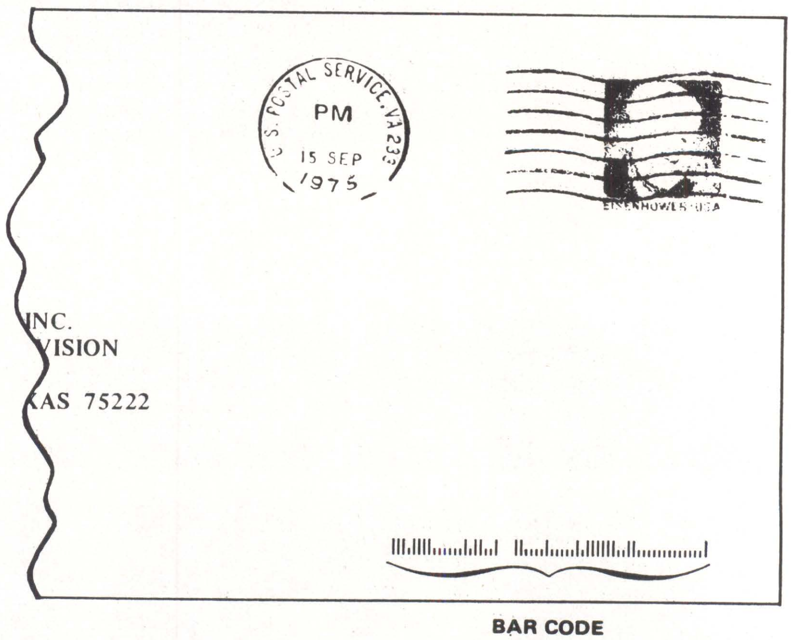
Surveillance and tracking telescopes will operate in tandem. Images will be displayed in standard TV format in the observatory control room from a camera mounted on the surveillance telescope.

Bar Code Reader Offers Improved Capability at Lower Cost

Patents covering a code-reading concept and hardware to implement a high-speed optical code-reading device have been granted to E-Systems, Inc, Dallas, Tex. The inventors claim the device will read any mail bar code the eye can see and at a lower cost than other code readers. Applications are predicted for both the U. S. Postal Service and high-volume mailers such as banks or utilities.

Heart of the device is an electro-optical sensor—an energy intensifier—which magnifies light 100 times to locate and "read" the bar code imprinted on the letters as they speed through mechanized mail sorters. Bar/half-bar address codes, printed on the envelopes either by the mailer or the Postal Service directly below the address or in the lower right-hand corner of the envelope, contain the street address, city, state, and ZIP code and provide the means for automated mail handling.

Because the reader is sensitive to all visible light, it can detect any imprinted bar codes visible to the eye. The reader first detects the presence of a code, then tracks it along the envelope even if it is skewed or slanted. It will also read bar codes correctly when ink smears between two bars or when handwriting inadvertently crosses through the code at 15 deg or more from vertical. Read speed of 275 in./s corresponds to 55,000 business-size envelopes/hr, or about 43,000 envelopes/hr through the mail-sorting system.



BAR CODE

Typical address bar code is usually printed in lower right-hand corner of envelope, as shown here, or directly below the address. Patented reader can detect and read any imprinted bar code that the eye can see, even if the code is skewed or smudged

Low cost disc storage for DEC, NOVA and Interdata mini's.

Compare the Plessey disc system (PM/DS) with those furnished by the original mini supplier. With the Plessey PM/DS you achieve double the storage in half the space at a big reduction in cost.

The PM/DS is software, hardware, and media compatible with the DEC, Data General, and Interdata family of minicomputers. It consists of a disc controller (PM/DC) and a dual disc drive (PM/DD) either of which may be purchased separately. The PM/DC will accommodate disc drives made by numerous manufacturers including Diablo, Wangco, Pertec, Caelus, and Iomec. The PM/DD contains five megabytes of storage, 2.5 fixed, 2.5 removable, and may be daisy chained in your existing disc system.

The PM/DS is another step in the Plessey plan to expand—from a leading manufacturer of minicomputer add-on memory, to a complete supplier of a wide range of mini peripherals. If you use DEC, NOVA or Interdata minis you can satisfy all your requirements for disc, memory, and punched tape products with one supplier—Plessey.

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Pattern Recognition Capability Lets Robot Operate Unattended

Claimed to be the first true production robot extensively employing visual image processing functions, a system has been introduced that can assemble a variety of types of transistors by means of pattern recognition techniques. Developed by Hitachi, Ltd, Central Research Laboratory, Tokyo, Japan, the system has been installed at the company's Takasaki Works for production of small and medium-sized signal-type transistors, eliminating the operator-manned wire-bonding process. Production rates have increased by more than twice that of more traditional operations.

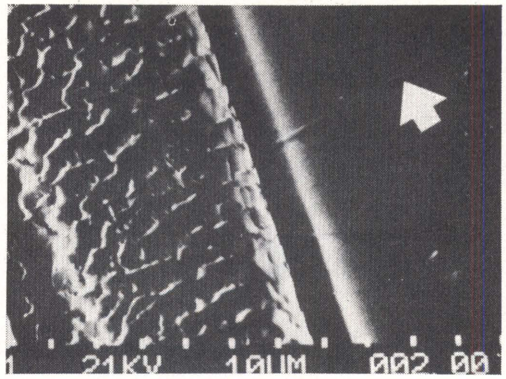
The system is made up of a minicomputer and image processors, and will ultimately have 50 wire-bonding machines with visual functions to determine chip positions of transistors fed into the machine. The computer, an HIDIC-150, has a 12K-word capacity memory.

To recognize the position of transistor chips, a microscope and a TV camera are mounted on each wire-bonding machine. Image signals from the camera are analyzed by a combination of the image processor and the computer. Average yield in high speed position recognition is 0.2 s/chip, at ±10-μm accuracy.

Recognized positional data are fed back from the computer to the appropriate wire-bonding machine. The data are used to position the high speed micro-servomechanism so that the wire-bonding mechanism on the servomechanism can stretch the gold wire between the emitter and the base electrodes on the chip and corresponding outer leads.

The transistor assembly system eliminates the most common bottleneck of automatic transistor manufacture. Completion of this system utilizing artificial vision is seen by the company as a step toward making the unmanned factory a reality.

Etching of 0.3-μm Line Widths Promises Improved Transistor Density



Scanning-electron micrograph of a just visible polysilicon line of 1-μm width (arrow) crossed by a human hair (the "rough" object on the left). The very narrow semiconducting lines are made by a special etching technique developed at the Mullard Research Laboratories, Redhill, England. (Figures at the bottom indicate the micrograph data)

Very thin lines for interconnections and transistor gates have been produced by preferential etching of polysilicon at the Mullard Research Laboratories (part of Philips Research), Redhill, England. Lines of 1 μm have been incorporated into transistors and still narrower (0.3-μm) lines have been made with cross-sections of only 600 x 600 silicon atoms. (Line widths in ICs are usually between 5 and 10 μm.) However, only conventional methods have been used in the laboratory experiments; no special apparatus is required.

The Mullard technique involves conventional definition of one side of the line with a masking layer on top. Boron is diffused into the edge of the polysilicon underneath the mask, to a depth equal to the width of the line required. The masking layer is then removed, followed by removal of the undoped region of polysilicon by a selective etch to leave the fine boron-doped line.

Widths of lines defined by methods such as photolithography, electron beam lithography, and X-ray lithography are directly affected by the roughness of both edges. However, in the Mullard process, line width is determined by diffusion from one edge and is little affected by irregularities in the original edge.

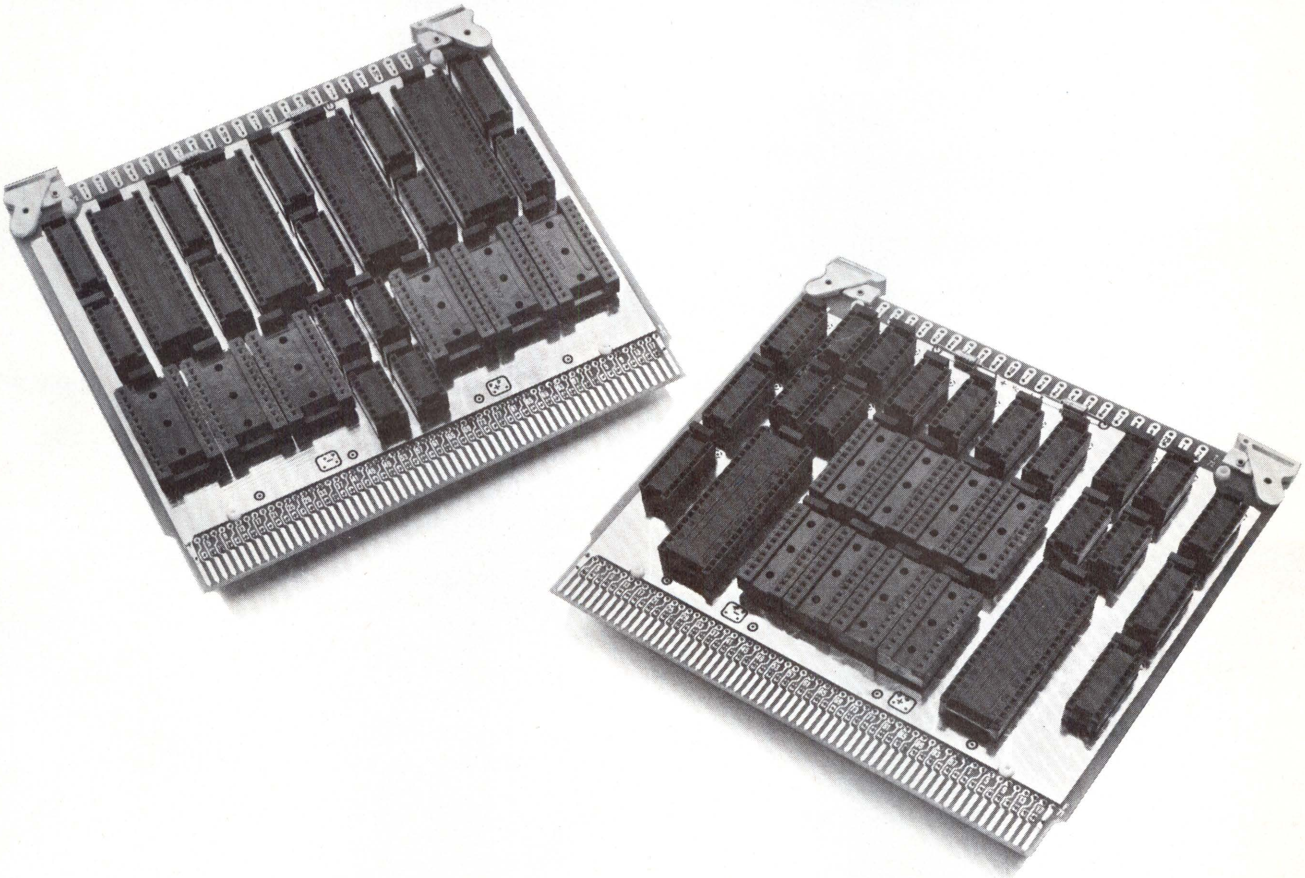
Transistor packing density is considerably improved by this technique. Ultimately, the cost of electronic circuits and products could be reduced. However, the results of these laboratory experiments do not necessarily imply a follow-up by Philips in production or marketing.

Spacecraft Processors Guide Booster Ascent and Control Attitude

A pair of general-purpose, on-board spacecraft processors, each weighing less than 8 lb and consuming only 5 W of power, can guide a booster into orbit as well as provide spacecraft orbital position information, according to an RCA engineer. The precise attitude control system is scheduled to be flown for the first time late this year aboard an advanced weather satellite being developed by the Air Force Space & Missile Systems Organization for the Defense Meteorological Satellite Program (DMSP). It was described by George A. Beck, a member of the program office of RCA's Astro-Electronics Div, Princeton, NJ.

Initially, the system is employed to place the spacecraft and its orbiting stage into a 450-nautical-mile sun synchronous orbit. By performing ascent navigation, guidance, and control tasks, the SCP-234 computers eliminate the need for a separate guidance computer and facilitate the use of the same inertial measurement unit for both ascent and on-orbit functions, according to Mr Beck. After achieving orbit, the computers maintain the spacecraft in its desired earth-pointing direction. Spacecraft position and velocity are calculated once every 0.5 s. The on-board computers utilize data provided by gyroscopes, a star mapper, and star ephemeris tables to assure a pointing accuracy of better than 0.1 deg. Position errors are fed into an attitude control module that enables the spacecraft to be repositioned as needed for precise pointing of the sensors. The processors may also be used for the on-board processing of sensor data and for handling equipment status telemetry information. □

New socket cards for microprocessors.

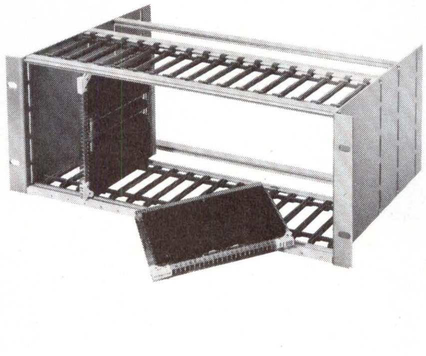


Instantly available, these two new cards are your answer to second-source problems. They enable you to change ICs and wiring for new pin patterns with great ease.

They are designed specifically for microprocessor applications, including controllers, random access memories, and erasable programmable memories. As such they are the newest in our line of 3D socket cards:

3D2017 Four 40-pin sockets, six 24-pin sockets, five 18-pin sockets, five 16-pin sockets, and four 14-pin sockets. $124.70.

3D2018 Two 40-pin sockets, eight 22-pin sockets, four 18-pin sockets, six 16-pin sockets, and eight 14-pin sockets. $140.70.



In addition, both cards provide a good ground plane for high-speed operation. They include a ceramic monolithic bypass capacitor at every socket, and provision for bypassing other voltages that may be required for chips. Power can be connected to various pins on LSI chips by means of solder tabs. And each card includes 22 built-in test points.

These cards are complemented by our line of Card-Pak card files, and our automated wiring service.

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The 990 computer family sets new price/performance standards because of an important milestone in MOS technology . . .

The TMS 9900 single-chip, 16-bit microprocessor.

Powerful enough to be the heart of a full minicomputer, the TMS 9900 is also the best microprocessor going for terminals, machine monitoring and control, and a host of OEM applications.

All in the Family

The same company . . . Texas Instruments . . . makes every member of the family, and makes every member software compatible, from the bottom up. The new Model 990/4 microcomputer and Model 990/10 minicomputer use the instruction set of the TMS 9900 microprocessor. This means that software developed for the low-end computers will be compatible with the higher performance models. And, users can expand their systems with a minimum of interface and software adaptation.

The TMS 9900 Microprocessor

The TMS 9900 is a 16-bit, single-chip microprocessor using MOS N-channel silicon-gate technology. Its unique architecture permits data manipulation not easily achievable in earlier devices. With its repertoire of versatile instructions and high-speed interrupt capability, the TMS 9900 microprocessor provides computing power expected from a 16-bit TTL computer.

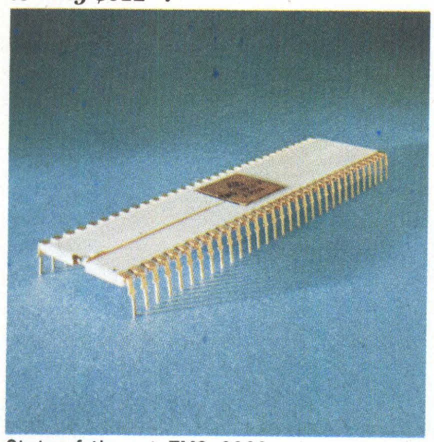
The Model 990/4 Microcomputer

It's a complete computer on a single printed circuit board using the TMS 9900 as its central processor. The 990/4 is ideally suited for terminal control, peripheral device interface control, and as a CPU for OEM customers.

In addition to the TMS 9900 microprocessor, the 990/4 microcomputer contains up to 8K bytes of dynamic RAM, up to 2K bytes of static RAM and/or PROM, eight vectored interrupts, front panel interface, real-time clock input, two I/O buses for low- and high-speed devices, and optional ROM utilities.

With the 990/4, you can select a low-cost OEM package, a 7-inch or 12¼-inch rack-mountable chassis, or a table-top enclosure . . . and memory expansion to 58K bytes.

Price: The Model 990/4 microcomputer with 512 bytes of memory is only $368* without chassis and power supply. This same model with 8K bytes of memory is only $512*.



State-of-the-art TMS 9900 microprocessor . . .16-bit, single-chip CPU with minicomputer instruction power.

The Model 990/10 Minicomputer

The most powerful member of the family is the Model 990/10 general-purpose minicomputer. The 990/10, a TTL implementation of the 990 architecture, provides the high-performance speeds demanded in many applications.

A memory mapping feature providing memory protection and privileged instructions supports memory expansion to two million bytes. And TILINE**, an asynchronous high-speed I/O bus, supports both high-speed and low-speed devices. Chassis options are the same as those for the 990/4.

Price: With 16K bytes of memory, chassis, power supply and programmer's panel, the Model 990/10 minicomputer is only $1968*.

Built Better Backed Better

In addition to the family of compatible hardware, Texas Instruments backs you with complete software and support. ***Standard software packages include memory-resident and disc-based operating systems;*** FORTRAN, COBOL, and BASIC compilers; and program development packages with utilities. And, for you to develop application programs for the 990/9900 family, we offer ***cross support on timesharing networks*** and standalone software development systems. One is a low-cost system using the 990/4 . . . the other is a disc-based system using the 990/10. And, a ***prototyping system*** is offered for TMS 9900 users to develop custom software and firmware modules.

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DIGITAL CONTROL AND AUTOMATION SYSTEMS

Computer Process Control Around the World

Sydney F. Shapiro
Managing Editor

IFAC 75, the 6th Triennial World Congress of the International Federation of Automatic Control, was held in Cambridge, Mass, Aug 24-30. Because of the potential interest to readers of *Computer Design*'s "Digital Control and Automation Systems" section, a review is included this month of papers involved with the use of digital computers in automatic control. (Papers that covered particularly new facets of the technology were abstracted last month—pages 46-50.) The December issue will contain a discussion of social/economic/governmental aspects of automation as viewed by IFAC 75 speakers. Considering that an automatic-control conference of this magnitude with speakers from so many nations will not be held for another three years, *Computer Design* believes this extensive editorial coverage is warranted.

Papers were presented by experts representing nearly all countries using automatic process control. Most were given in English, but language problems were evident in the oral presentations and are noticeable in the printed versions of the papers. However, those interested in particular subjects will likely have sufficient knowledge to manage an understanding in spite of the sometimes crude translations.

Man/Computer Interface Problems

An extremely important aspect that must be considered by the system engineer designing a computerized process control system is the man/computer interface. Many processes have historically been fully man-controlled. To expect that operators will simply accept computer control is naive. Not only will operators naturally oppose changes to their set routines, but there is an inherent "fear" of computers as a threat to job security.

In the adaptation of computer control to processes that for decades have been controlled manually,[1] thorough consideration must be given to both the challenge to operator ego and the reluctance to change ingrained procedures. Otherwise, successful implementation of a process computer control system is not likely to be realized. One of several suggested key solutions is to build in procedures which allow the operator to use his experience rationally to confirm computer calculations—to make his decisions important to the system. The operator's confidence in the system will build when he is permitted to see and review all the facts. There is less likelihood that he will be tempted to revert to haphazard instincts.

Development of Process Control Systems

Evolution of computer control in extensive or complicated processes has been relatively slow and tortuous. In the early stages, a single, large central computer was used to control a major portion or even all of a process, with a number of on-site controllers time-sharing the mass storage. Complexity and cost of interfacing and programming were monumental and most potential users were discouraged from implementing such systems.

With the advent of hierarchical systems, however, many of the drawbacks were removed. Programming was still involved and costly, but the overall systems were much more dependable and efficient. Also, both computers and peripheral system components were now less expensive.

If one of the remote-control computers became inoperative, it did not shut down the entire system. Because even the supervisory computer could be much smaller and less expensive than the earlier, large central computer, a system designer could include a redundant processor to fill in if the master computer failed. In addition, many systems were designed such that the remote computers contained sufficient capability to permit continued operation of system components even if both master computers failed.

Current tendencies are toward even more efficient systems with microcomputers at most control points. These can be dedicated to specific control functions, with a supervisory minicomputer handling many microcomputers—and a medium-size central computer supervising a number of minicomputers.

Iron and Steel

One trend is to bring whole plant complexes or even entire companies under unified coordination and control. In the iron and steel industry, for example—one of the first to make widespread use of computers in controlling its processes[2]—such implementation could be very effective.

Automatic control of a modern steel mill requires monitoring of a vast number of different variables operating under a very wide range of process dynamics. A large number of complex relationships must be translated and, if necessary, corrected. Such control corrections must be transmitted to a very large set of widely scattered actuation mechanisms. All of this involves the expenditure of extremely large amounts

New From Tektronix– A High Performance Logic Analyzer

- MORE STORAGE
- MORE RESOLUTION
- MORE VERSATILITY
- LOWER COST PER BIT

The new LA 501 Logic Analyzer from Tektronix provides 4096 bits of storage. Front panel selectable storage formats range from 4 channels x 1024 bits to 16 channels x 256 bits to accommodate your specific application. Sampling rate to 100 MHz (10ns/bit) insures the resolution necessary for analysis of high speed logic. Timing diagram readout provides maximum data density in a format close to real time operation.

Other outstanding features include pre-trigger operation for viewing over 90% of the stored data before the external trigger, compatibility with all logic families, vertical movement of any selected channel for easy timing comparison with other channels, both horizontal and vertical magnification and movement of the display for detailed viewing of a segment of the data, and a choice of internal or external clock for asynchronous or synchronous sampling of machine data.

The LA 501 is housed as a plug-in for the TM 500 Series of test and measurement instruments. This means you can combine it with your choice of plug-in display, oscilloscopes, multimeters, counters, signal sources, and digital delay in a system tailored to your specific application.

For maximum flexibility, the LA 501 interfaces with any x-y display having at least 500 KHz bandwidth. If an oscilloscope is used for the display, it can be used for further electrical troubleshooting once the fault has been located.

At only $3250, the LA 501 with its large storage capacity, high resolution, convenience, and versatility is your best logic analyzer buy.

For complete information, contact your local Tektronix Field Engineer or write: Tektronix Inc., P.O. Box 500, Beaverton, Oregon 97077. In Europe write: Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

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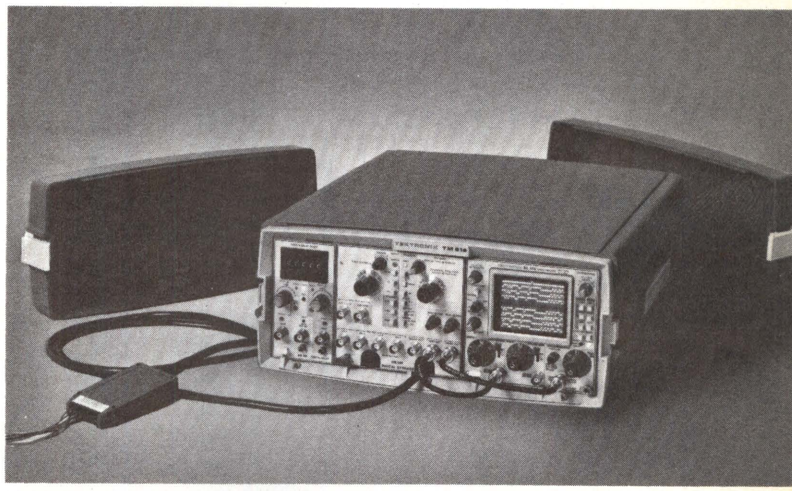
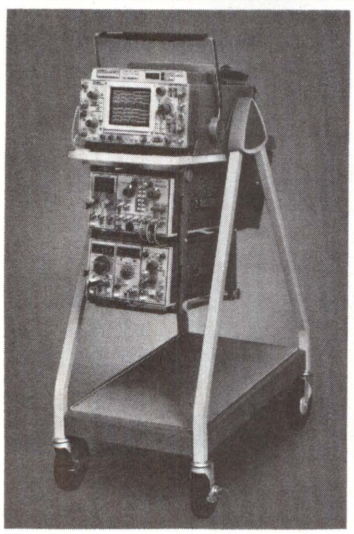
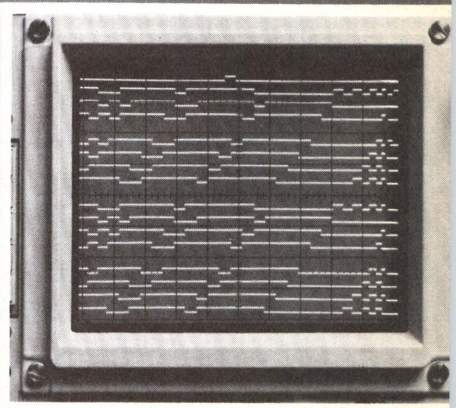
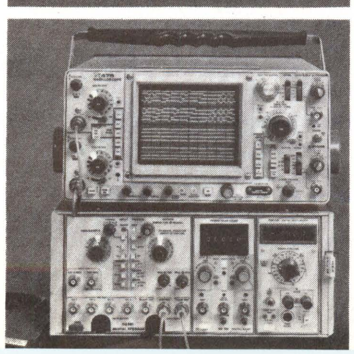
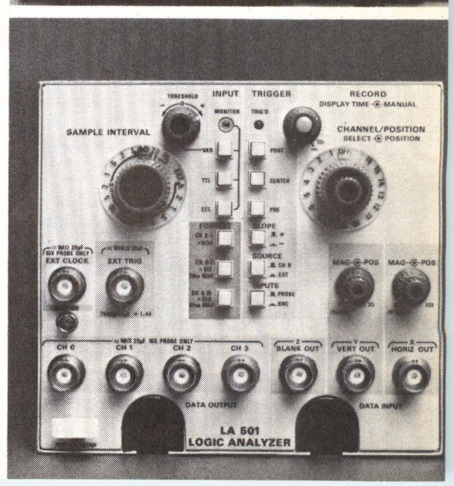










of energy. Not only should computer control increase productivity, but major savings in the massive energy requirements should be achieved by better coordination of operations of the successive units in the production line.

Chronology of the evolution of computer control in the iron and steel industry is typified by events in Japan.[3] The first phase, in which one analog computer supervised the control of setpoints through a number of analog controllers, began in 1965. Major portions of the process were "controlled" by a single computer, but the levels of control were limited and man was often a part of the feedback loop. Sophisticated function sequences or multi-step control sequences could not be controlled at acceptable levels of expense. In addition, it was difficult to improve accuracy beyond that of the analog controllers.

In phase 2, which began about 1970, analog controllers were gradually replaced by programmable controllers and digital computers (Fig. 1). Direct digital control was introduced and the control functions could now be more than merely supervisory. Sophistication of control began to evolve. Since control logic was in software, changes could be made more readily, stability levels of control were raised, and—because more control loops could be handled by a single computer—relative cost was lowered. Probably the most important result, however, was standardization of the computers. System designers no longer required manufacturers to supply "one-of-a-kind" computers.

However, serious problem areas still exist. One computer handles many control loops and very high reliability is required; a failure involves many loops. Since computer access is time-shared, it is difficult to realize real-time control. Also, the increase in software complexity necessitates the addition of many more software engineers.

Phase 3, with the advent of minicomputers in hierarchical systems, is expected to ease many of the problems. More work will be accomplished by relatively inexpensive hardware, and software will be simpler. Individual digital controllers—which might be microcomputers—will need to control fewer loops and, therefore, reliability will increase. Higher sampling rates will provide faster control. Real-time control will be feasible since time-sharing will not be necessary in maintaining control of individual loops. Sophisticated control, however, will still be feasible by combining the

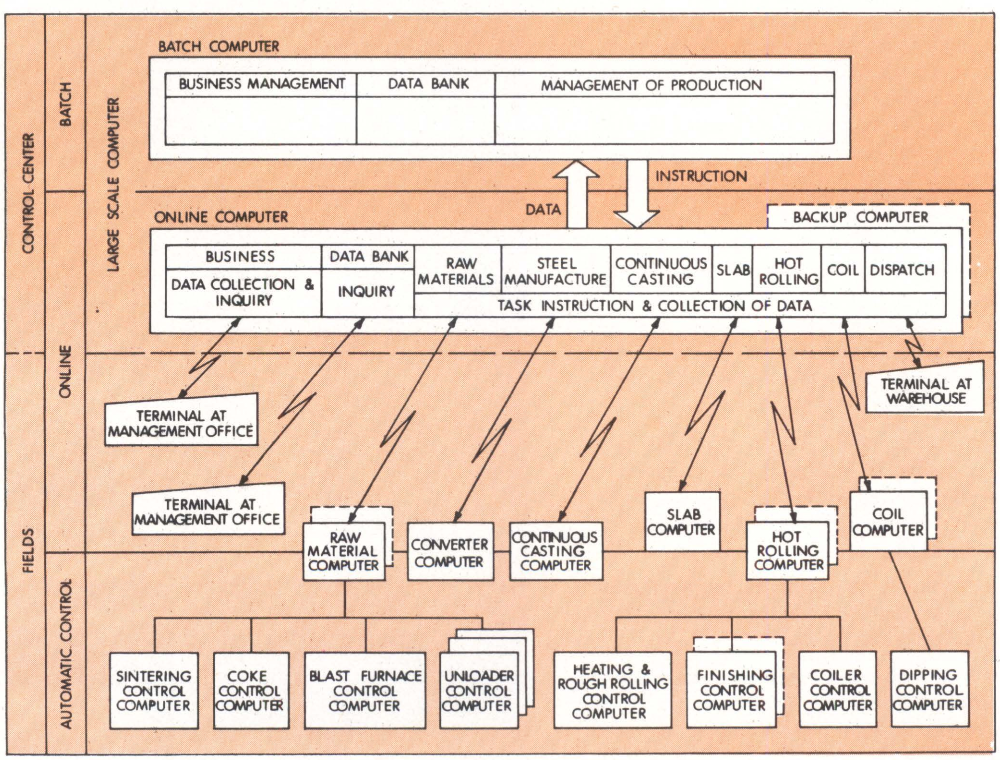


Fig. 1 Example of direct digital control of a steel plant with computers used in all production phases.[3] Low level system is automatic control, middle level is online, and high level is batch. Introduction of microcomputers will provide faster sampling and, therefore, faster control. In addition, it will reduce the amount of communications cables required

Without our communication interface devices, micros would have nothing to talk about.

How to turn a micro into a conversation piece.

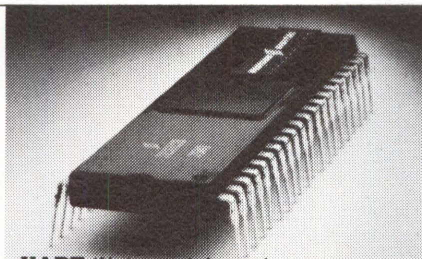
In simple terms, our communication interface devices (CIDs), help micros and peripherals communicate with each other. Without CIDs, the best micro would be speechless. A fact that may startle all those who think that micros are the hottest thing since minis. The point is, a micro is only good for something if it's hooked up to our CIDs–the chips that make a micro work within a system.

Five ways to make a micro open up.

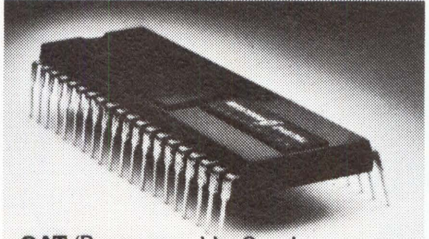
Our bright engineers came up with a whole family of CIDs: MOS/LSI UARTs, SATs, SARs, ASTROs and FIFOs, our First-In First-Out Data Buffers. All of these devices share a number of advantages. Each is so dense, it can do the job of many. Each is compact and costs substantially less than what you had to use before CIDs. And all of them cut down power consumption. Drastically.

ASTRO–the makings of a star.

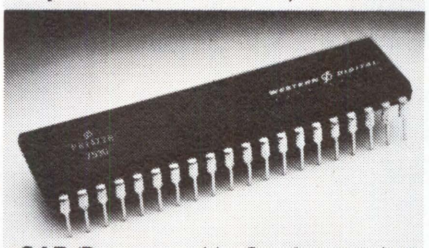
We're particularly pleased with our ASTRO. It's the CID that's an Asynchronous/Synchronous Transmitter/Receiver all in one chip. The ASTRO is IBM bisynch compatible (systems compatibility is another typical CID characteristic). It can replace as many as 50 chips in one computer-based system. 32 ASTROs can be addressed on a bus. No wonder everybody in the business wants them. A lot of them.



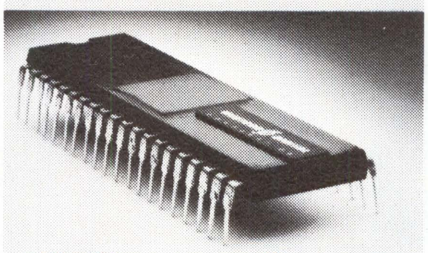
UART (Universal Asynchronous Receiver/Transmitter)



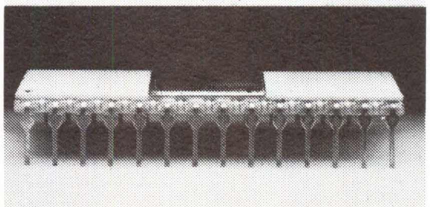
SAT (Programmable Synchronous/Asynchronous Transmitter)



SAR (Programmable Synchronous/Asynchronous Receiver)



ASTRO (Asynchronous/Synchronous Transmitter/Receiver)



FIFO (First-In First-Out Data Buffer)

How one chip leads to another.

Now people are looking forward to our first SDLC–a Synchronous Data Link Control device. That shows that our customers expect a lot from our engineers who were the first to anticipate the need for all kinds of CIDs. We haven't disappointed them yet.

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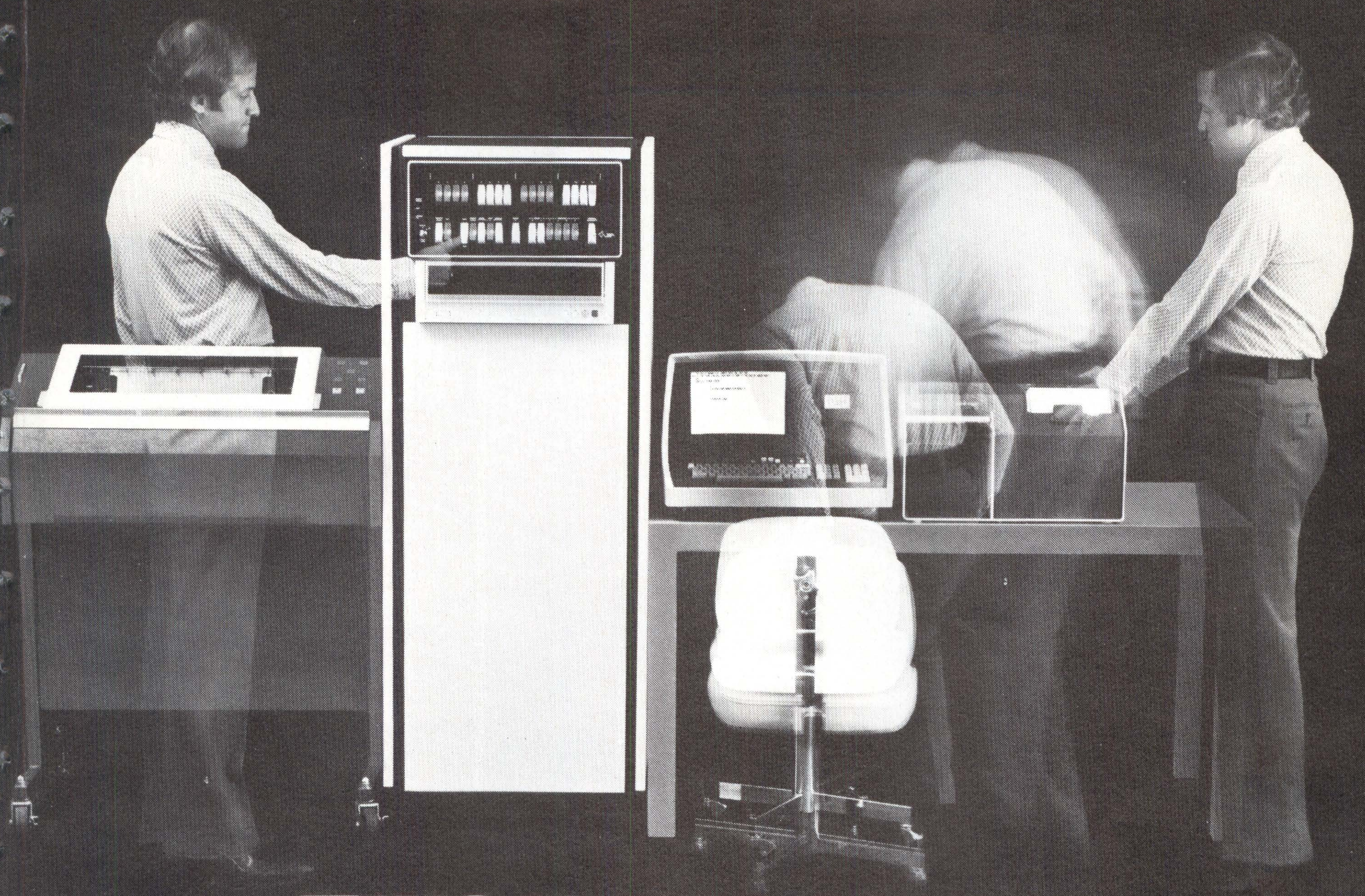

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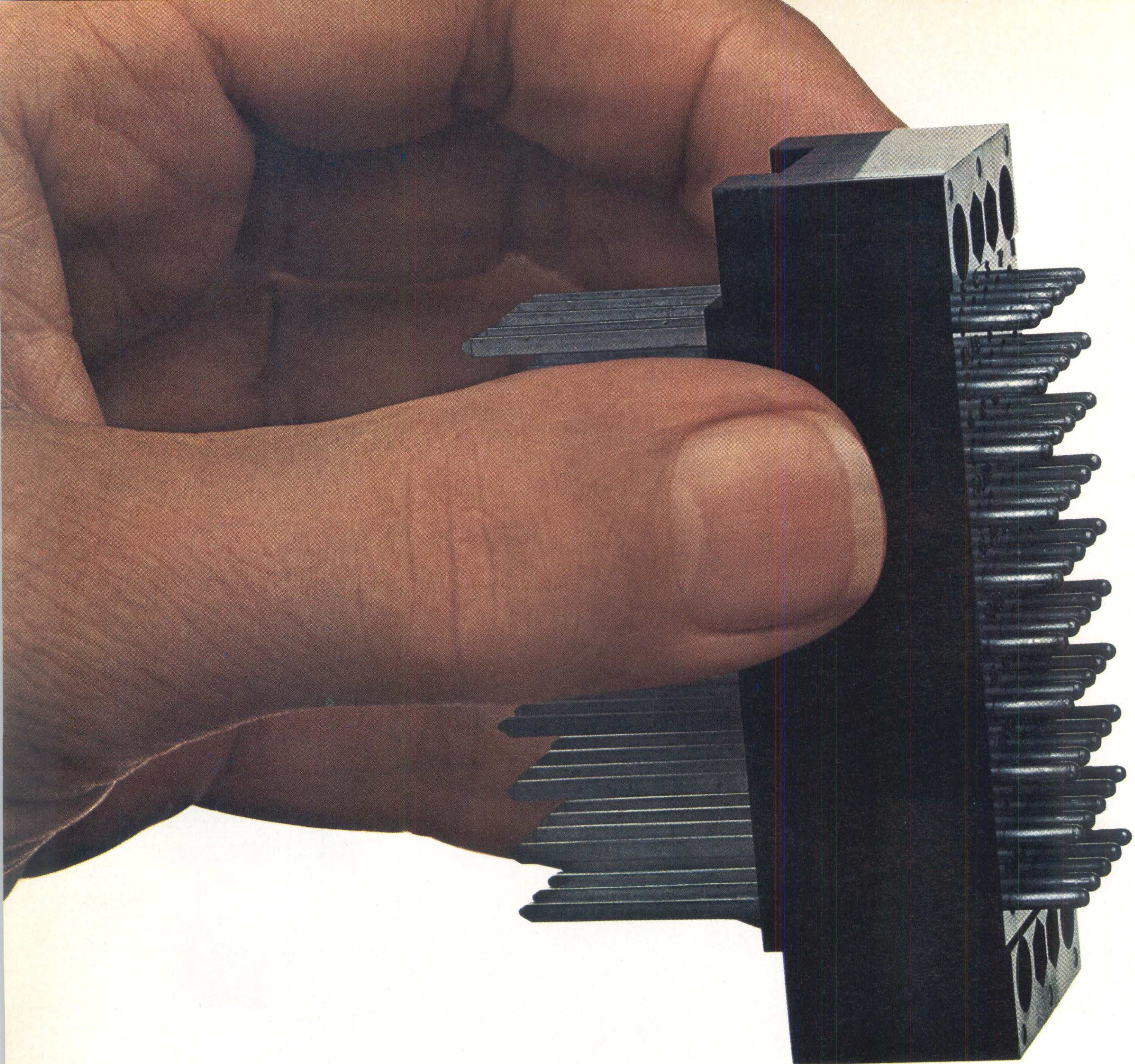

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It's available with either point-to-point or crimp snap-in contacts.

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CIRCLE 35 ON INQUIRY CARD

minicomputers (and microcomputers) with supervisory process control computers.

Problem areas do remain—particularly concerning available sensors. In most cases these instrumentation problems can be solved through computation from more accurate process models. However, it is conceivable that some steps will not be fully automated until more reliable or more accurate sensors are invented.

No doubt the current trend toward hierarchical systems will ease many of the design pains that have existed in the past. Use of large-scale integration electronics will possibly even aid indirectly in solving some of the sensor problems. It is likely that extremely reliable multicomputer, hierarchical control systems can be developed to automate most of the functions of a modern steel mill.

The advent of the microcomputer will probably increase rather than decrease dependency on software engineers, particularly since in very large complexes software will be distributed to a number of locations. At least one paper, however, did note some question on the adaptability of microcomputers to the environmental conditions of the iron and steel industry.[3]

(A Frost & Sullivan market study of digital control sales in the 1974-79 period forecasts that sales of U.S.-manufactured digital controls to the iron and steel industry will increase from $19 million in 1974 to $32 million in 1979. For all process industries, the leap will be from $280 million to $514 million. Of these increases, microprocessor controllers are expected to show the largest rate of growth by far.)

Computer Control Systems in Other Industries

Examples of the application of digital electronics to solve control problems in other process industries illustrated economic or production gains that could not have been otherwise attained. The following digests of these systems are intentionally brief. Readers interested in detailed discussions may find them in the published Proceedings.

Automatic Measurement and Control of Wood Logs.[4] Two fundamental areas of information must be determined when processing wood logs for industrial use: geometric dimensions and qualitative parameters. At present, only dimensions are automatically measurable; qualitative parameters still require the human factor. In the system discussed, logs are transported by chain longitudinal conveyors at speeds up to 100 m/min., stopping at a check point for measurement. An optimal cutting decision is made for each log and lengths of appropriate pieces to be cut are set up automatically by a displacement measuring system. The computer determines the optimal cutting decisions from information supplied by transducers and from the operator. It then controls operation of the crosscut saw and sorting of the pieces of lumber. (For a discussion of a related system for measuring and sorting green lumber, see *Computer Design,* July 1974, pp 52-54.)

Batch Cooking Plant.[5] "Cooking" is a chemical operation which processes wood chips into unbleached pulp. Chips are mixed in a reactor, or "digester," with cooking liquor heated by steam. Because steam consumption of each digester varies widely, every di-

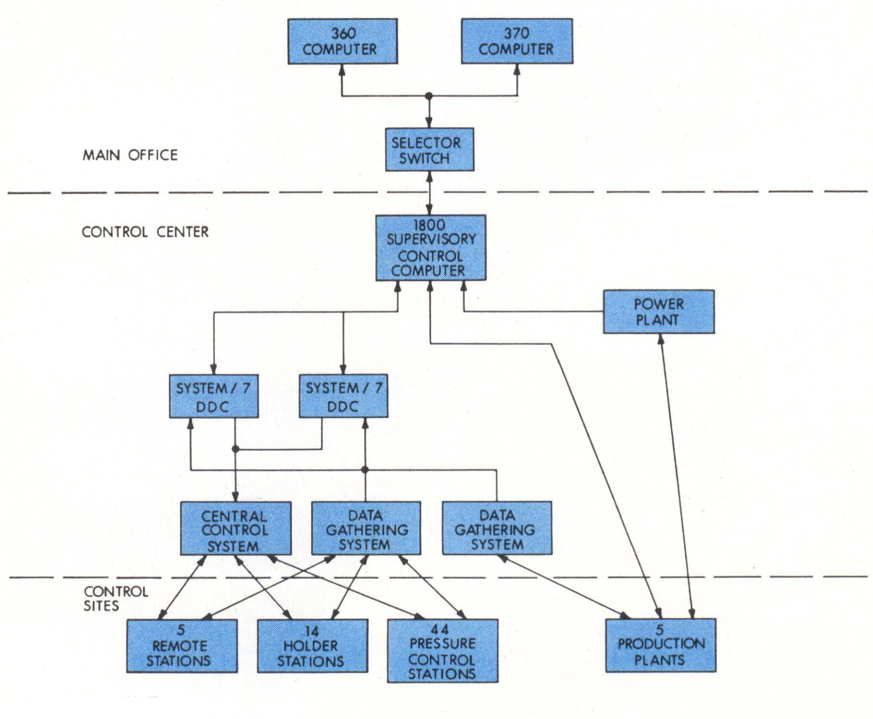
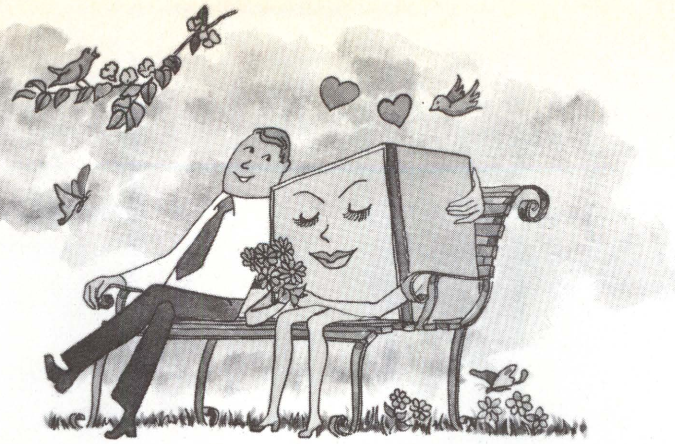


Fig. 2 Simplified block diagram of multi-level hierarchical control system for production and distribution of city gas.[8] In addition to the computers shown, supervisory control computers located in the production plants interface with small DDC computers in those plants.



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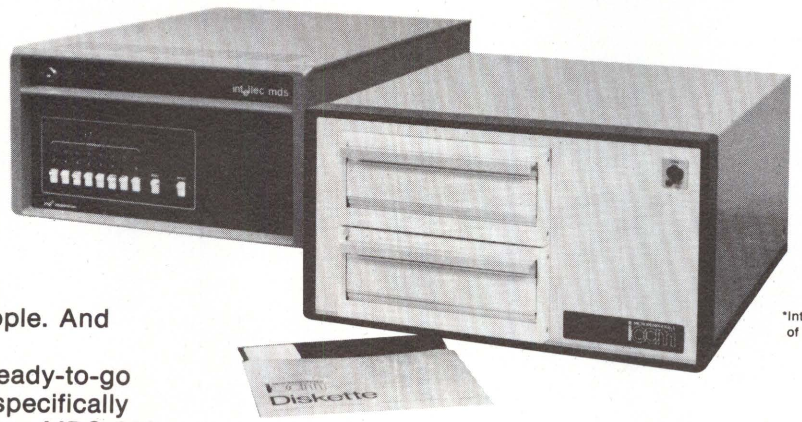

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The iCOM FD360 Floppy Disk System connects easily to the Intel MDS-800 through our interface card which plugs directly into the MDS chassis. The interface card is furnished with a PROM pre-loaded with the floppy disk driver software. You also get the cable which connects the interface card to the iCOM Floppy Disk System. You might say we've thought of everything.

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The controller/formatter portion of the system is fully IBM 3540 and 3740 format *and* media compatible. Special features include separate read & write data buffers, hardware track seek & verification, and complete hardware CRC generation & verification. Storage capacities range from 256K bytes to over 1 million bytes.

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A single drive system, including all software and the MDS interface card, is just $2650. The dual drive system is only $3300. And delivery is 2 to 4 weeks! We also have a 250 cps paper tape reader (Model R80MDS) for just $895. So why wait? Call or write today for more information. The sooner you order your iCOM Floppy Disk System, the sooner you can "turn on" your Intellec MDS-800.

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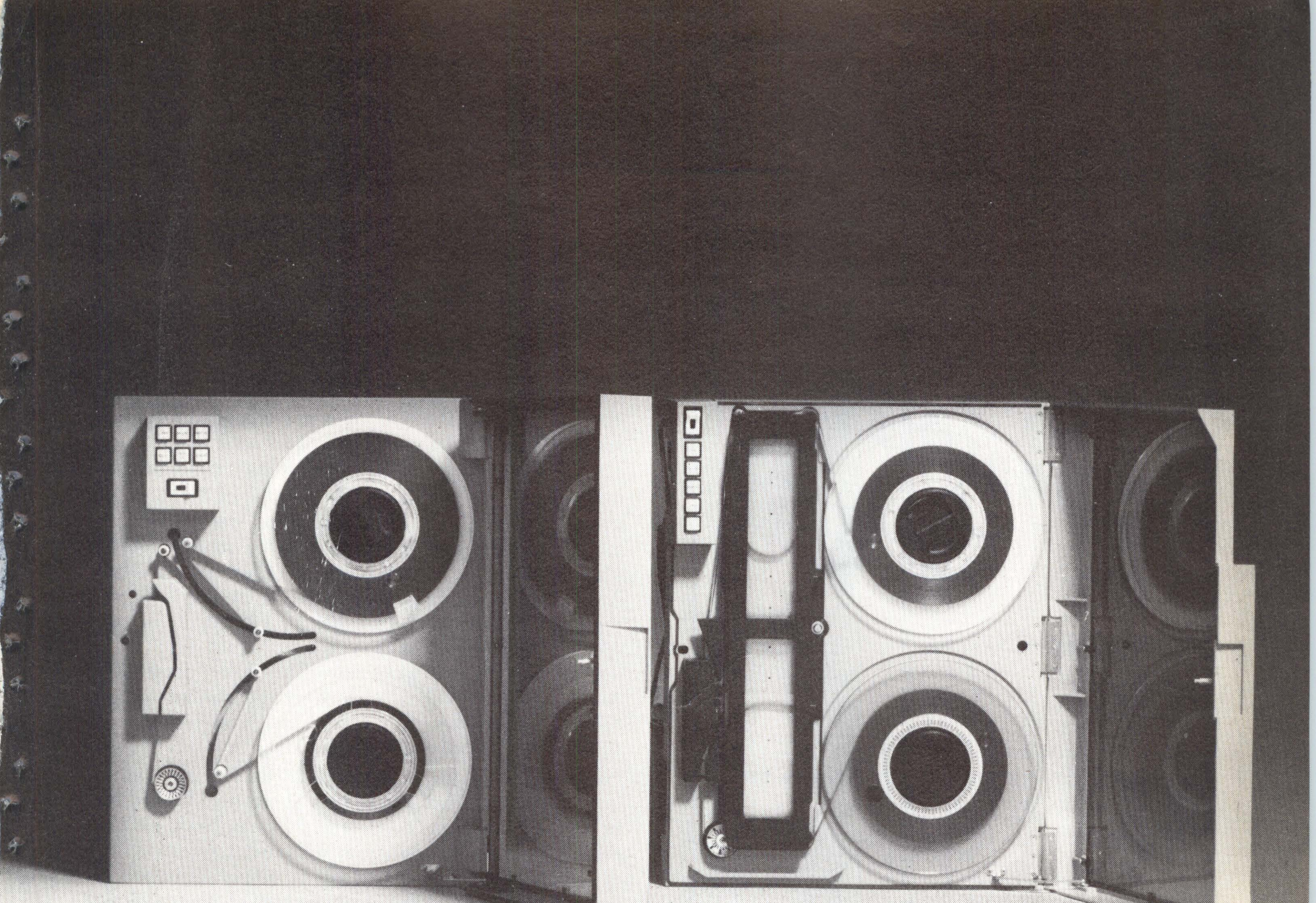

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We have 24-hour emergency service. (7 days a week.)

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And we have the largest and most extensive direct sales and service organization of any independent computer peripheral company in the world. (Over 40 Pertec Service Centers.)

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We take the risk out of buying.

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And, to top it off, our customers get a service resource that is one of the largest, most available, and fastest in the industry. With direct and factory-trained service representatives worldwide.

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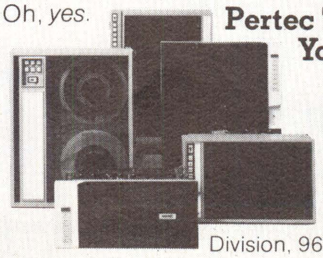

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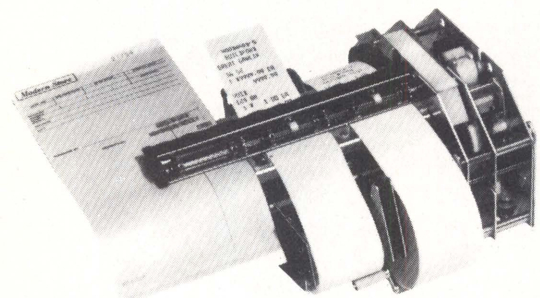

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unique segment matrix character format

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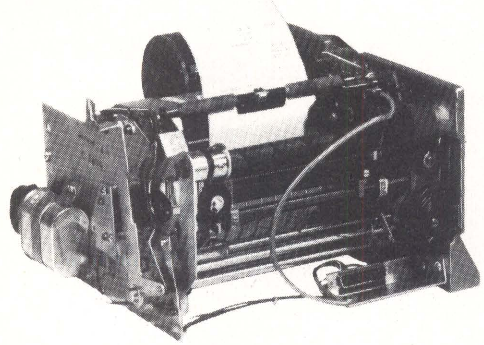

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30–column serial printers

Two models, each with different external dimensions for greater applications flexibility. Print up to 44 alphanumeric and special characters. At 37 characters per second. Can print on unit front inserted forms. Journal take-up spindle provided.

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CIRCLE 37 ON INQUIRY CARD

gester cycle disturbs the electrical and thermal equilibrium of the entire mill. The study reported was on determination of an optimal control that would minimize the variations in total steam consumption. Two optimization algorithms were worked out: nonlinear, with cascade solving of constraint conditions, and hierarchical calculus. Requirements for the two methods, respectively, were 11K and 19.5K of memory, 0.25 s and 0.5 s of computing time without disturbances, and 0.5 s and 1.2 s computing time with disturbances. The first algorithm is presently being programmed.

Galvanizing Line.[6] Maintaining both uniformity and weight of the zinc coating added to steel during the galvanizing process is critical in order to meet quality standards and to reduce the cost of excessive coating. A fully automatic computer system in use by U.S. Steel regulates inline annealing through control of line speed during a continuous hot-dip process in which the steel is coated with zinc. The coated strip then passes between "knives" which are controlled by the computer to maintain the required edge-to-edge and side-to-side zinc-coating thickness.

Potassium Dressing Plant.[7] Both fluctuations in ore quality and complex production processes are involved in the formation of potassium chloride. Such steps as grinding, desliming, flotation, thickening, filtration, and drying require rapid evaluation of online measurements as well as fast response with corrective control action where necessary. The system discussed involves a Soviet Union plant in which an ASVT M-3000 central computer system performs both evaluation and control.

City Gas Production and Supply.[8] A computer hierarchy consisting of large, medium, and small computers is being used for total control of both production and distribution of liquified natural gas (Fig. 2). IBM 360/65 and 370/155 computers (one for backup) are located in the head office. These communicate with an IBM 1800 supervisory control computer (SCC), which in turn interacts with a number of IBM System/7 direct digital control (DDC) computers. Some of the five gas production plants also contain SCC and DDC units for local control. Older instrumentation and feedback control routes are analog; however, more sophisticated control steps require DDC. Provision has been made for even greater expansion of the control system, using all digital techniques. Process operations are now performed at speeds several times faster than possible by human or analog control.

Soda Plant.[9] Multiprocessor, non-hierarchical control using 16-bit minicomputers provides necessary flexibility in this system. Four ASVT M-6000 computers serve in separate tasks but also allow full redundancy (Fig. 3). If one computer fails, its functions are performed by another of the processors. Steps are performed in real time.

Automatic Fare Collection.[10] Ticket sales, ticket checking, and gate control at station entrances and exits are performed under a 3-level hierarchy in the Paris urban Metro network. Three levels of equipment are involved: station peripherals, fare collection processing, and data collection. Standard telephone cables laid in the railway tunnels connect the first and second levels; a multiplexer working on a computer channel-to-channel link connects levels two and three. The system, progressively being put in operation since the end of 1973, will eventually handle all stations in the railway system. At present it includes about 2000 station peripherals, but capacity exists for double that number. (See *Computer Design,* Sept 1974, pp 60-64 for discussion of a related system in use by Illinois Central Gulf Railroad.)

Automated Warehousing.[11] Heavy bundles of H-section steel beams of varying size and cross-section are moved, stored, and retrieved automatically at a Nippon Steel Corp plant. When bundles of beams leave the rolling mill, information concerning configuration is sent to the computer. Each bundle is then checked at a confirmation point and a label attached. All bundles under 15 m in length move into the automated warehouse. Duplex central processing units as well as other major parts of the computer system assure full-time operation; if a master unit fails, its backup counterpart assumes control. Each central processing unit is a Melcom 350/30 with 32K words of core memory. Four 256K-word magnetic drum memories, 26 peripheral devices, and nine operator consoles are also in the system. A higher level, supervisory computer performs overall production control—from order acceptance to shipment.

Robotics

Relatively small stress was placed on robotics at the Conference. Only one session paper was specifically related to the subject.[12] This involved a laboratory experiment for a hand-eye, minicomputer-controlled robot

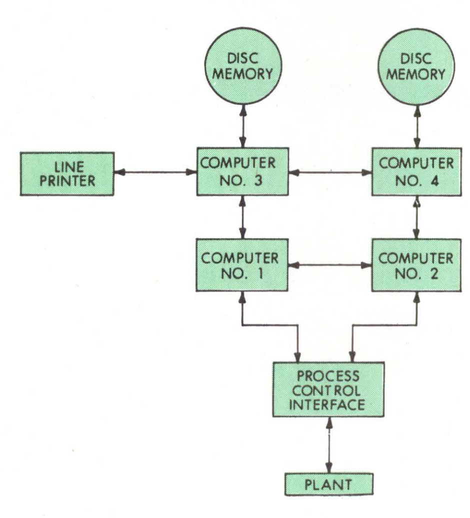

Fig. 3 Configuration of multiprocessor computer system for process control of a soda plant.[9] As many as 24 soda production units may be connected

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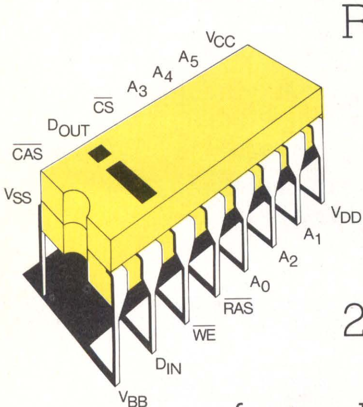

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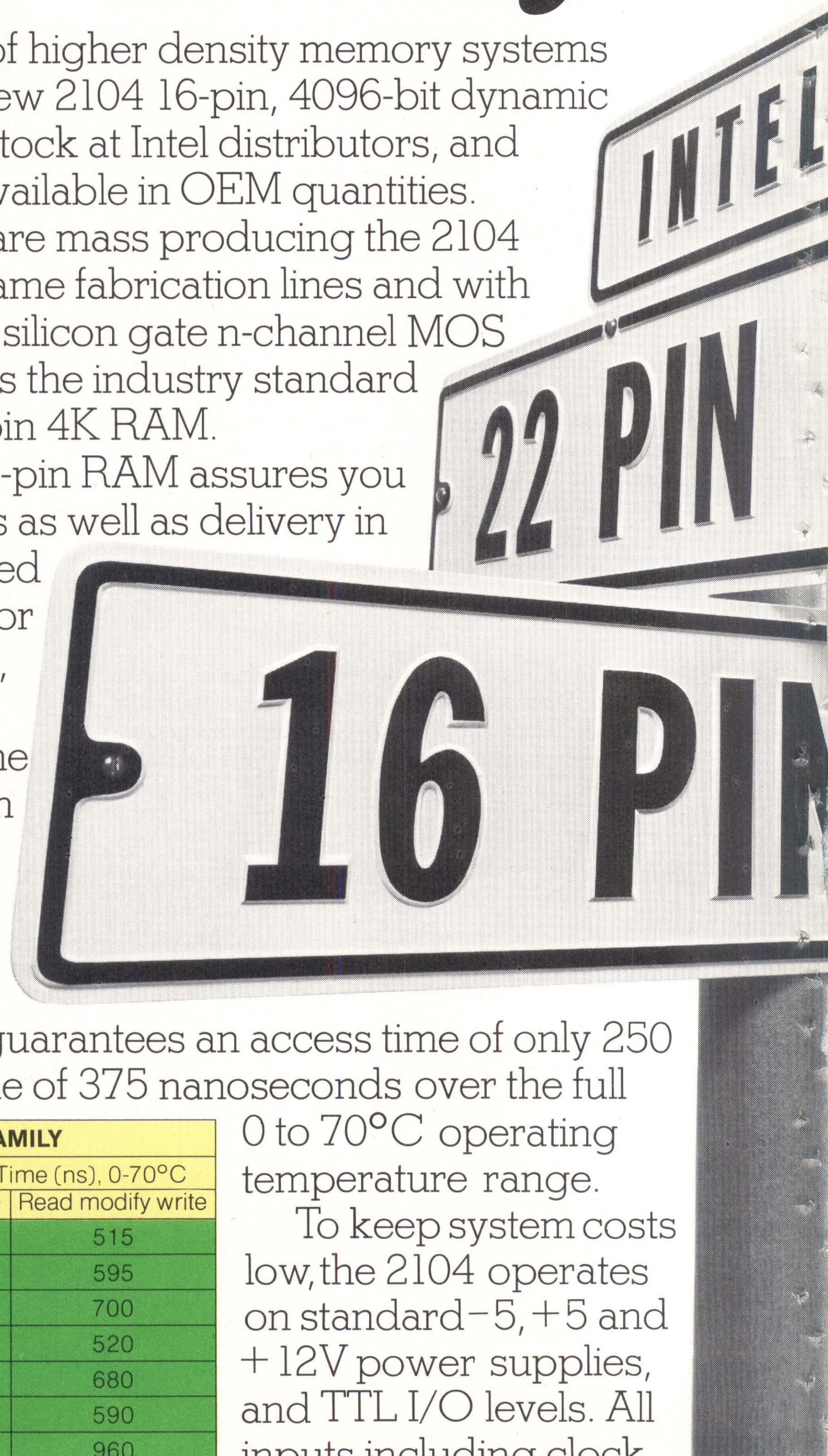

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D2104-4	16	300	425	595
D2104	16	350	500	700
2107B	22	200	400	520
2107B-2	22	220	470	680
2107B-4	22	270	470	590
2107B-6	22	350	800	960

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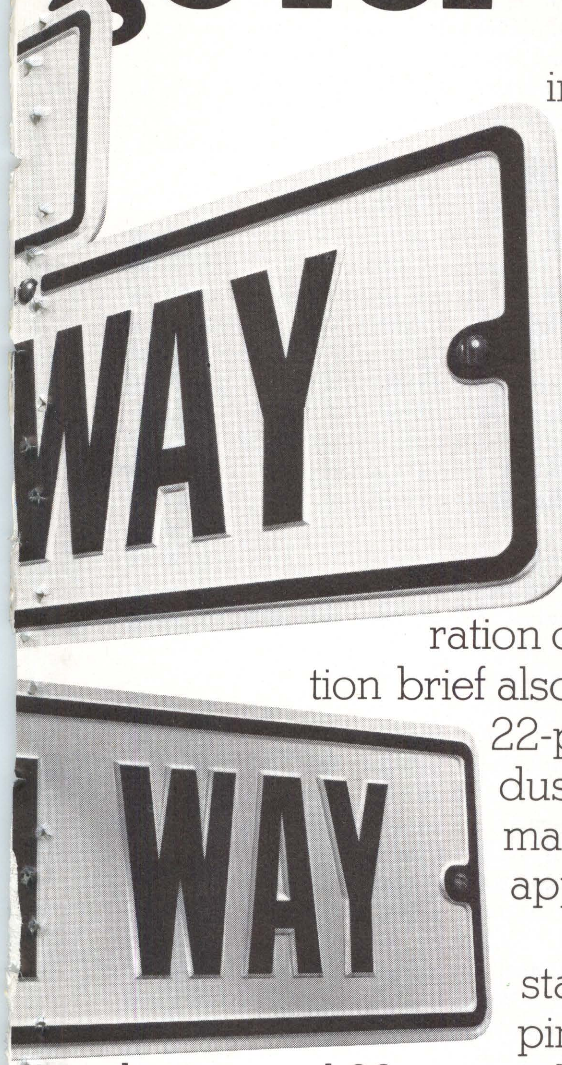

inputs are fully TTL compatible.

Overall system advantages of the 2104 are detailed in a new application brief, "Which Way for 4K... 16, 18, or 22 Pin?" It explains why the 16-pin 2104 is best for very compact systems such as minicomputers, microcomputers, terminals, business equipment, scientific calculators and anywhere high density is needed.

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that will integrate state-of-the-art technology with practical applications. Although intended to be put to use as soon as possible, design of the "Budapest robot" is such that new—even contradictory—ideas can be incorporated.

A CII 10010 minicomputer was originally planned for the system, but the present unit incorporates a 16-bit Data General Nova 1200 with 16K words of core memory and a 2-megabyte disc. Man-machine interaction is provided by a display that can visualize the recognition phase, eg, contours. Laser beam illumination provides very accurate detection of 3-dimensional features. Parallel-acting photodetectors placed in various locations note direction of movement. A screen before the photodetectors, calibrated for the laser's wavelength, provides a display that is adequate for operation in full daylight.

First-level description of an object is a list of picture primitives, ie, lines, arcs, nodes, and undefined elements. Extraction is common and unified in all cases. The list is the foundation for the second level, which consists of generalized picture primitives. These are simple but characteristic substructures containing two to five primitives, and are fixed for a given pattern class. Recognition and description are performed by grammatical analysis. Quantitative attributes permit their use in synthesizing higher level structures.

The third level consists of lobes, each of which is an unordered list of generalized picture primitives contained by a given object. A lobe is highly characteristic for an object. However an object may have several lobes with different probabilities as a result of noise, shadows, or other disturbance factors. In a learning phase, therefore, the system constructs the field of conditional probabilities of lobes by which a given object can be identified.

In recognition phase the heuristic program issues a list based on the learned conditional probabilities and the "measured" lobe actually being displayed. This tells the organizer program which objects or groups of objects are most probably being displayed. By this procedure, the system avoids the need to search through the entire memory of structure identification and can concentrate its determination in the direction of highest probability.

The fourth level consists of synthesizing the object's geometric structure, based on only a few well-defined details. This structure is defined only by relations between quantitative attributes of generalized picture primitives. All other details can be located relative to the coordinate system defined by attributes of the generalized picture primitives.

(Although not yet involving visual recognition capabilities, experiments at the University of Virginia have advanced beyond the minicomputer stage to the use of microcomputers. For a general discussion of the technology, see "The Role of Microcomputers in Robotics," by K. Goksel and E. A. Parrish, *Computer Design*, Oct 1975, pp 56-71. In addition, a real-life, online use of visual recognition by a robotic device is reviewed this month on p 54.)

Experiments with legged locomotion robots were discussed in one of the Plenary Sessions.[13] Because of the subject's specialized interest, this paper is not abstracted here. However, the full text is included in the Conference Proceedings.

Direct Digital Control

First implemented about 10 years ago, direct digital control (DDC) is not yet a trouble-free technology and certainly not a universal solution for all operating problems.[14] DDC in the digital process control environment is the "technique of controlling a number of process variables from one digital computer, programmed with selected feedback or feedforward modes." In effect, this is total plant control. Intervals for sampling each controlled variable are so small —1 s for flow control, 5 to 30 s for most other loops —that the dynamic characteristics of the process are masked.

A major deterrent to implementing DDC in more processes appears to be lack of economic justification rather than technical feasibility. Although in some plants DDC can be put to use simply by replacing analog control elements with their digital equivalents, in most cases this does not provide operating cost advantages. Total plant control by computer will be economically justifiable only when the full ability of DDC is used in a plant designed to take advantage of all the inherent capabilities. This will require implementation of such features as feedforward, adaptive, or multi-variable control; process evaluation and diagnosis; automated startup and shutdown; and process optimization.

Many processes must automatically stop if the control computer fails. In a control configuration of full plant complexity that was wholly dependent on a single computer, failure of that computer would result in financial disaster. With a dual computer system, however, a backup computer assumes full control if the primary computer fails. This redundancy increases mean time between failures to an acceptable figure. In hierarchical systems, if one of the several computers controlling different portions of the overall process fails, only that portion controlled by the failed computer will shut down. Even then the supervisory computer may be able to assume control if another technique for redundancy is not incorporated.

(Many DDC systems, both for individual process lines and complete plants, are now operational. For some examples, see *Computer Design*, 1975: Apr, pp 56-60; July, pp 50-54; and Sept, pp 46-53.)

Microcomputers

Admittedly, one of the deterrents to placing many more control systems online has been cost. Even minicomputers, in some cases, are too expensive. Entrance into the era of the microcomputer, however, is eliminat-

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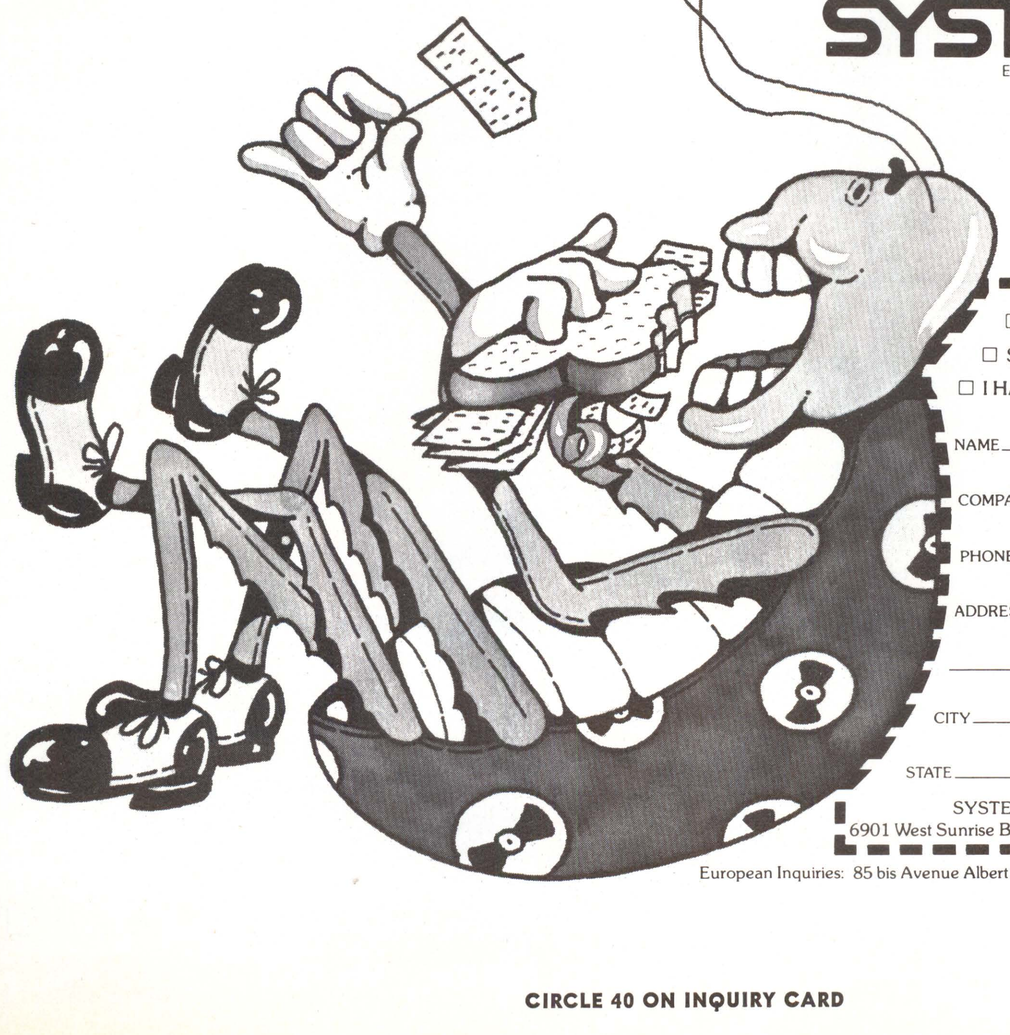

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ing this holdback for most installations. While certainly not universal panaceas, microprocessors (CPUs) and microcomputers (CPUs plus memory and input/output interface) will likely permit digital control to be instituted in a great number of processes not now automated.

One speaker, however, pointed out a drawback that must be considered seriously: because of the small size of many of the systems that will soon be under digital control for the first time, these systems will often interact with nontechnical people.[15] Care must therefore be taken to be certain these sysems are reliable and easy to use.

Seemingly, the control application areas for microcomputers are endless. (See *Computer Design,* Oct 1975, pp 49-50 for an in-depth discussion of a double processor system.[16]) One area where computer use for online control has been limited in the past is in nuclear reactors. However, the microcomputer may change this if a current experiment is successful. A thermal, open pool reactor under analog control was used as a test vehicle.[17] In this case, in order to make a fair comparison, microcomputer DDC was used with the same input and actuator as the analog controller (Fig. 4). No changes were permitted in either process or instrumentation.

The 1-MW research reactor—with 93% enriched ^{235}U core and peak neutron flux of 4×10^{13} neutrons/cm^2/s—is used for experiments requiring neutron or gamma radiation and for training of nuclear reactor operators. Control requirements are automatic control of reactor power from 10 W to 1 MW, regulation of reactor power within 0.5%, automatic power increase at constant period up to 1.3 decades/min., automatic power decrease as limited by the reactor dynamics, and automatic turning of "square" corners on reaching a desired power level. Safety requirements include instant disengage from automatic control if the operator attempts to insert or withdraw the regulating rod or when any of several specified reactor conditions occurs, audible alarm on entry or disengage from automatic control, and a number of other detection or monitoring points.

Each of several control modes uses proportional control but most require additional control to give satisfactory response. It was found that, after transients have died out, the control system holds power within ±0.2%.

CPU for the modular computer hardware is an Intel 8008-1 microprocessor. Four kilobytes of read-only memory are used for program, coefficient, and data table storage; and 256 bytes of random-access memory are used for input, output, and intermediate variable storage. Input/output (I/O) circuitry is straightforward, with a device decoder used to decode and engage multiplexers for the I/O modules.

Software also is modular, with each self-sufficient module performing a specific real-time task. A main module links all the functional modules to form a system.

It was determined that microcomputer control of the reactor showed an improvement over the previous analog controller. In addition—and even more important—several new functions were provided by use of the microcomputer: operator-oriented displays, dynamic feedforward for wide-range operation, system safety checks, system self-diagnostics, and maintenance aids.

Summary

Automatic control has become an accepted procedure and the digital computer is now assuming predominance over analog controllers in broad leaps. Early problems of cost, slow response due to time-sharing, and operator reluctance have been largely eliminated. Com-

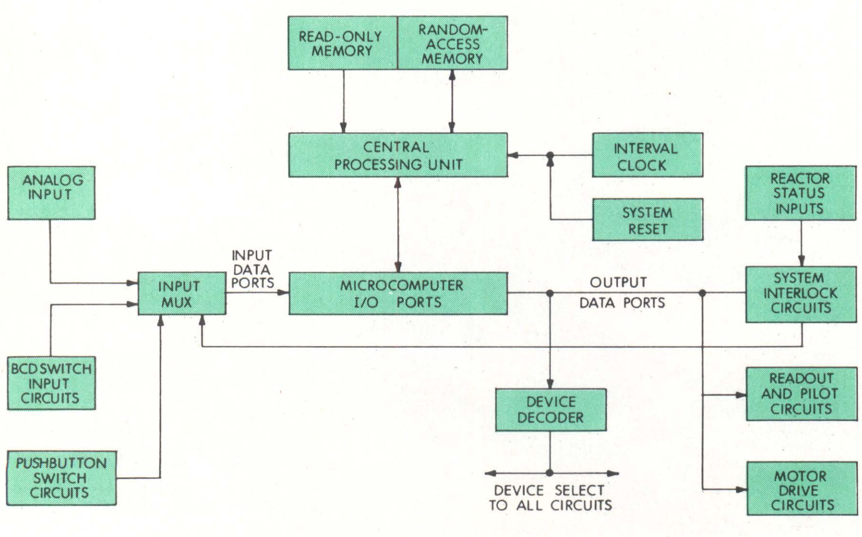

Fig. 4 Hardware interface functional block diagram for microcomputer control of 1-MW open pool reactor.[17] DDC not only improved control over that of a previously used analog controller but also provided several new functions

puters have become more standardized, and much smaller, less expensive units can be used. Hierarchical systems based on minicomputers have eliminated the need to time-share and have provided true real-time control.

Although the microcomputer has to date been applied to relatively few systems, it is likely to have a tremendous influence on future designs. It is cheap, it is reliable, and it is readily assimilated. By the next IFAC World Congress—in 1978—it is likely that microprocessors will be universally used in control systems. However, this will not eliminate the use of minicomputers. It will, in fact, increase the use of minicomputers as supervisory controllers in place of present large computers.

References

All references are to papers presented at IFAC 75, to be published in four volumes: I—Theory, II—Applications, III—Systems, Economics, Management, and Social Effects (also includes Plenary Session papers), and IV—Computers, Space Components, and Education. (Copies may be ordered from Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222, USA, or John Wiley & Sons, Ltd, Baffins Lane, Sussex PO191UD, England. Payment of $35 per volume or $125 for the complete set of four volumes should accompany order.)

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2. Purdue University Steel Industry Project Staff (USA), "Hierarchical Control Systems in the Steel Industry," Vol III, Paper 12.1
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17. R. A. Smoak and H. D. Scott (USA), "A Nuclear Reactor DDC Using a Microcomputer," Vol IV, Paper 20.5 □

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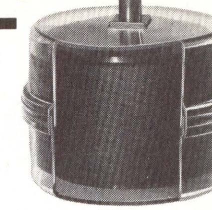

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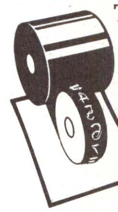

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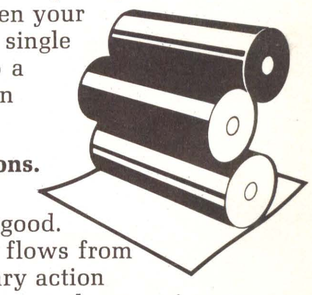

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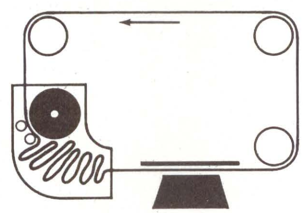

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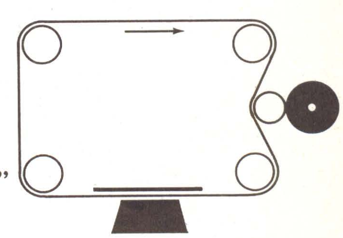

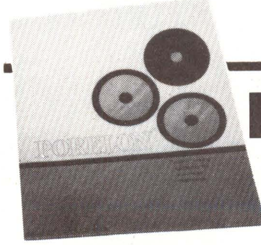

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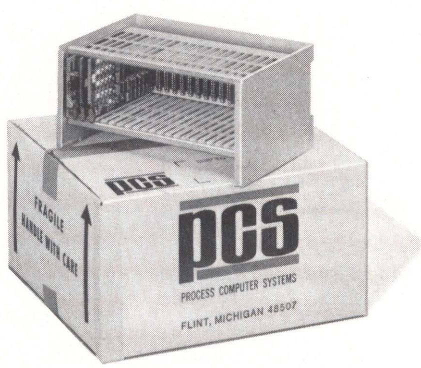

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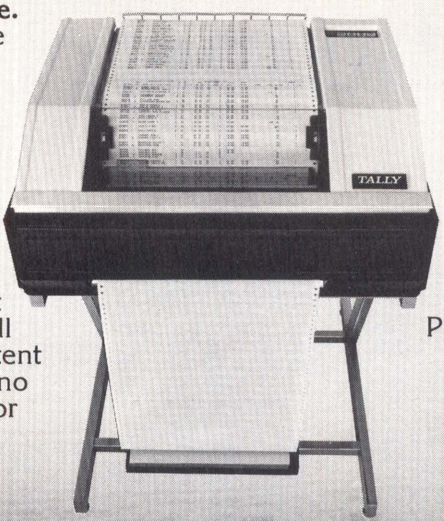

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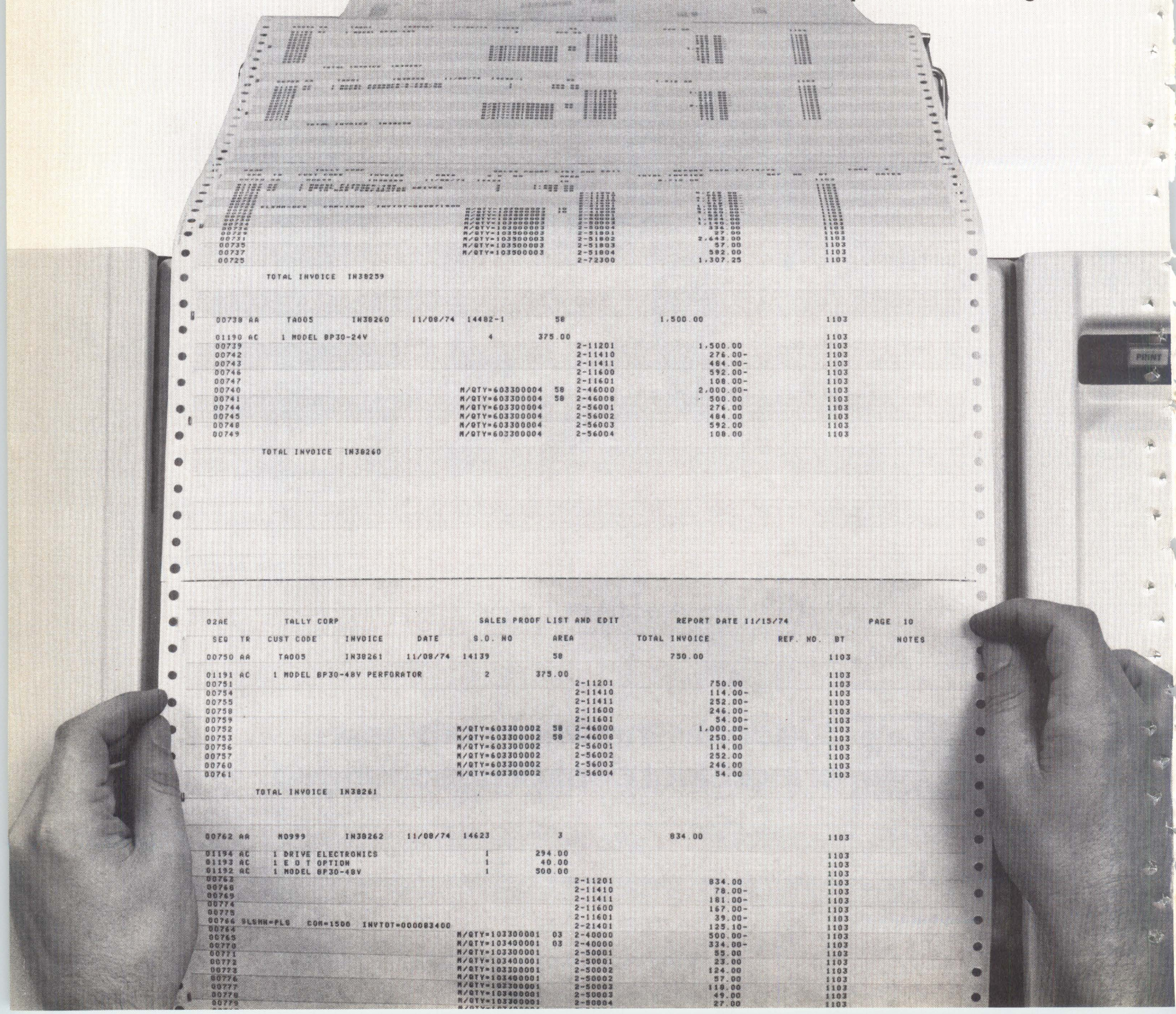

Traffic congestion in the storage systems of large computing centers—a growing and potentially very serious "hot spot"—can be efficiently controlled at low cost in a new approach to storage system design

A New Approach to Network Storage Management

James E. Thornton, Gary S. Christensen, and Peter D. Jones

Network Systems Corporation
St. Paul, Minnesota

A system has been designed which directly addresses the problem of managing a large number of storage devices with increasing traffic—a configuration that is becoming more and more common in centralized computer installations. With a special-purpose processor and a serial coaxial trunk, it improves performance of the entire system and permits further growth more easily than does the conventional system design. One key feature is that no single unit in the system ever has control, which means that no single unit can create a bottleneck in the flow of data, and no single-unit failure can bring down the whole system. The design represents a fresh approach to system architecture, utilizing existing equipment more efficiently at large cost savings.

One type of installation where this concept can be of value is the large system that delivers service to terminals connected by telephone lines. This mode of operation provides small, individual users with the economies of scale that are inherent in large computers. However, development of these systems has demanded a parallel development of large, permanent storage subsystems for user data, which also permit economies of scale to be made available to the small, individual user.

An examination of the capacity of storage needed in this new environment, however, exposes a quite serious problem: how to manage the large number of storage devices with increasing traffic. Most operators of large installations now recognize that this must be solved before they can provide added service. Their best solution so far has been to assign one host processor the task of managing the shared storage devices (Fig. 1) This processor executes the file management system—a task that includes space allocation, indexing, and cataloging—and transfers data to and from the host processor(s). Although this configuration performs well,* it is very expensive and likely to be inadequate for growth at a single site.

In contrast, the new system design (Fig. 2) is geared to very high traffic, significantly outperforming the large, conventional configurations. The high performance local communications network can also be applied directly between front-end processors and the host computer.

The system's serial coaxial trunk transfers data at 50 megabits/s. A matrix of such trunks provides a nearly unlimited number of connections among the storage devices and host processors.

Adapters between the trunks and individual devices convert parallel data to serial form and vice versa, and modulate and demodulate the serial waveform at the interfaces between processor, storage unit, and cable. The adapters also contain temporary buffer storage, permitting an effective match between the speed of the connected unit and the speed of the cable. For example, a disc unit transfers one block of data into the adapter at 6.8 megabits/s. The block is held in the adapter's buffer for an error check, following which the buffer is emptied into the cable at 50 megabits/s.

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*R. J. Mancini, "Performance Analysis for the Skylab Terminal System," *IBM Systems Journal*, Vol 2, 1974

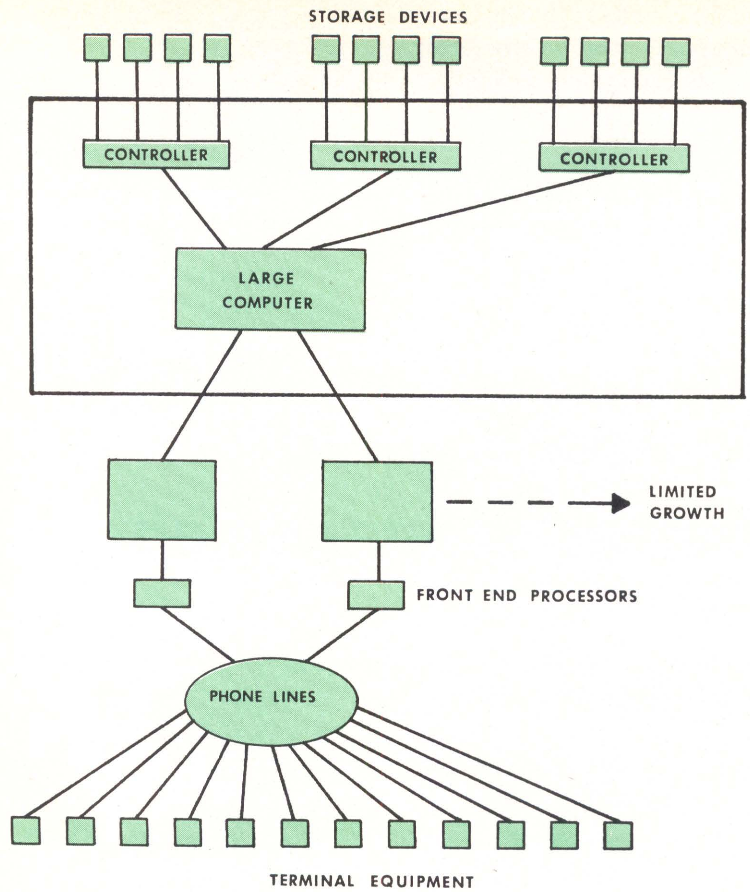


Fig. 1 Conventional system. An array of magnetic disc drives in large computing centers is commonly controlled by a single, large computer that manages all units for the remaining processors on the site. This approach can bring down the whole system when the storage-management processor fails; it is expensive and inefficient, creates a bottleneck for the flow of data to and from storage, and presents difficulties when the system is expanded

A similar speed translation is made in the computer data channel adapter, so that a device can be attached with an instantaneous data rate greater than that of the channel. In addition, with double buffering in the disc adapters, high speed computer data channels can block-multiplex data from a number of discs concurrently without degrading disc performance.

One coaxial cable can interconnect up to 16 processor or storage units separated by as much as 1000 feet. The special-purpose processor, called a network control unit, can manage 16 such cables. With these capabilities, over 200 units can be interconnected at a simple site. Of course, most sites demand redundancy, which is provided by running the relatively inexpensive network control units in tandem.

SDLC "Plus"

One significant advantage of a high speed serial line is its ability to connect to literally any computer or storage device. The interface adapters, in addition to their conversion, modem, and storage functions, convert the serial signal to the proper parallel interface, regardless of the manufacturer of the device. Such a "transparent" interconnection requires a network protocol; the one chosen is a variation of IBM's synchronous data-link control (SDLC) (see Table), which has been proposed as an industry standard.

Standard SDLC is an "electronic envelope" into which a data message is placed. The transmission medium uses this envelope, which contains a source and destination address, to transfer strings of data bits of varying lengths without regard for the content of the data. In the new network system, this link control requires the destination unit to respond to the source after every message, so that all transfers are interlocked, block by block.

In the Table, the fields marked by asterisks are essentially identical to the proposed standard. The three added fields include an access code, a FROM

Frame Format

*FLAG	8 Bits
Access Code	16 Bits
*TO	8 Bits
FROM	8 Bits
*Function/Status	16 Bits
Header Checkword	16 Bits
*Data	n Bits
*Data Checkword	16 Bits
*FLAG	8 Bits

*Same as standard SDLC

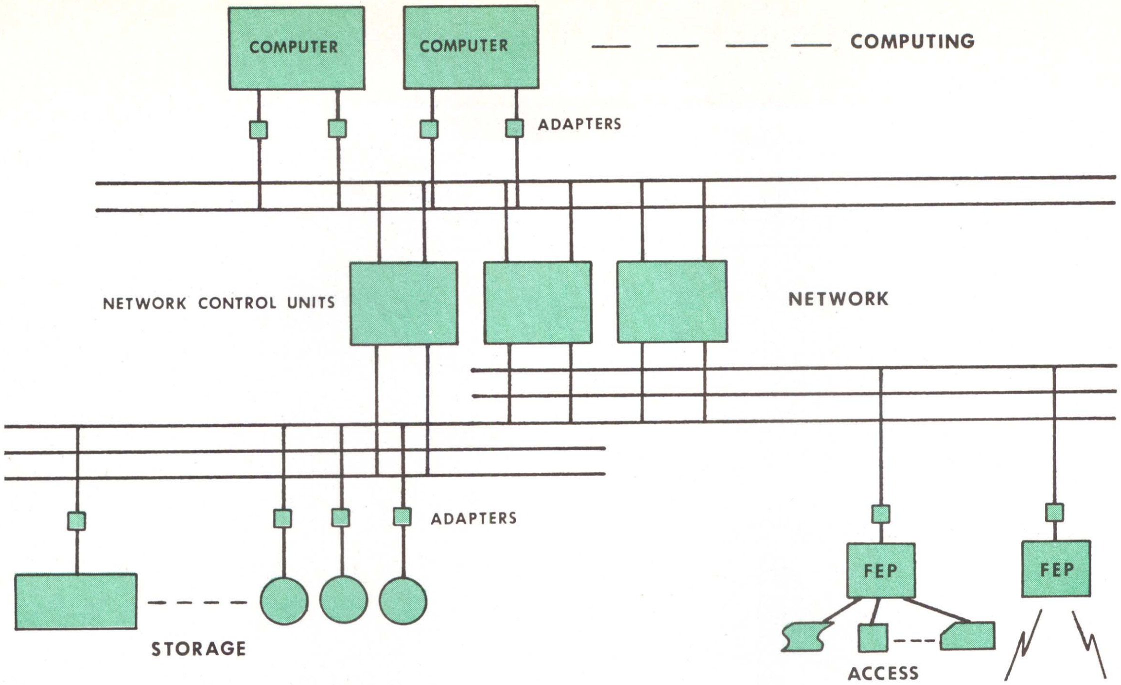


Fig. 2 New approach. Higher efficiency and low cost can be realized when the components of a system are interconnected through serial cables, in a network controlled by a special-purpose processor

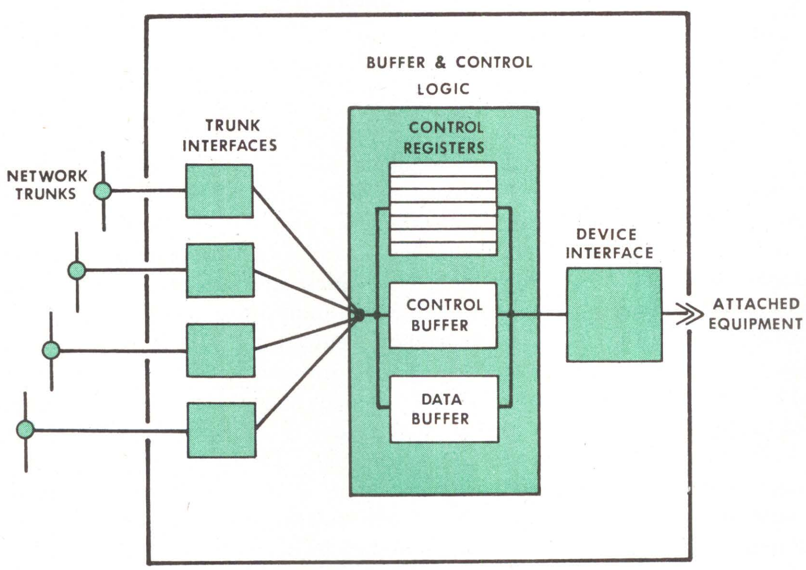


Fig. 3 Network adapter. One or more serial trunks are connected to conventional parallel devices through an adapter that converts the data, checks for errors, preprocesses the message, and communicates with peripheral controllers or processor channels

address, and a checkword following the header, Standard SDLC assumes a single circuit connection from source to destination, either hardwired or established in advance of transmission by a dial-up procedure or equivalent. In contrast, the network has a continuous structure that does not use circuit switching; therefore, the access code is necessary. Since a given link can have more than one source, the FROM address is necessary.

Finally, a checkword on the header is important, so that if the header is faulty, the transmission does not continue wastefully through a useless data field, but instead can be aborted while recovery of the header is attempted. In accordance with standard SDLC, the data have their own checkword that follows their transmission.

Interface Adapters

Each connection to one or more coaxial trunks within the network is made through an interface adapter (Fig. 3). Each trunk interface contains the 50-megabit/s transceiver, serial-to-parallel and parallel-to-serial logic, the checkword sync code, and access code logic. An adapter can contain more than one trunk

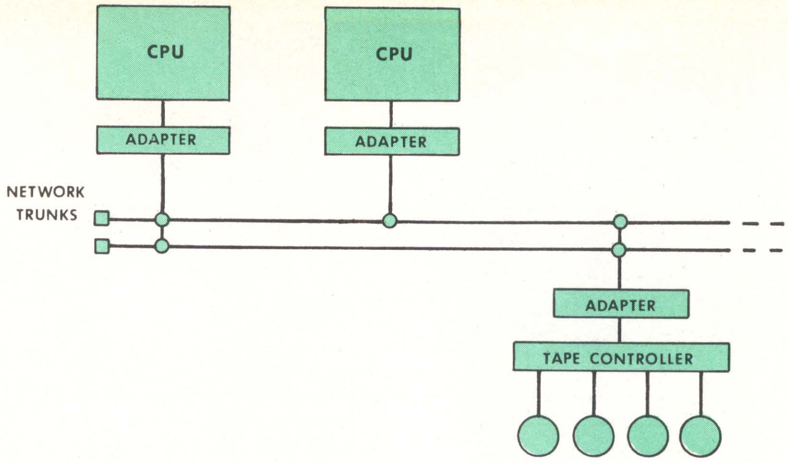


Fig. 4 Mini-network. Adapters alone can control some interconnections, provided the network topology is not too complex and little or no simultaneous interconnection is necessary

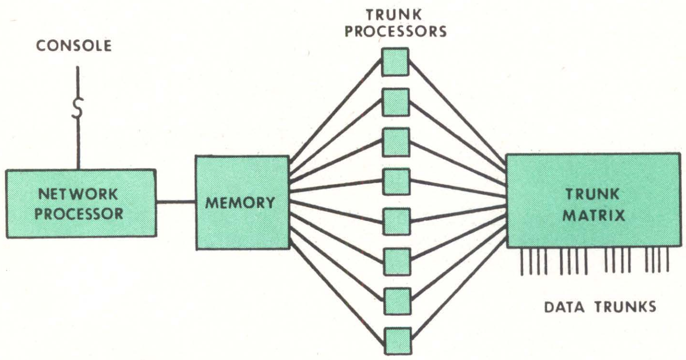


Fig. 5 Network control unit. For realistically complex interconnections, this unit oversees all operations. Processor is a fast 16-bit unit; memory has 8-way interleaving for the trunk processors. Trunk matrix is the crossbar switch through which the unit communicates with up to 16 trunks

interface, thereby acting as a channel switch. In case a trunk interface is using an adapter when another trunk interface attempts to transmit into it, the second trunk receives a busy response.

All trunk interfaces in a single adapter are connected to a single buffer memory and control logic section, which are common to all trunk interfaces. With the buffer memory and registers within the control logic, an interface adapter can perform sophisticated functions on the messages under control of a processing unit.

Each interface adapter has a hardware section defined as the device interface. In this context a device may be a processor or its standard channel, or it may be a storage device or controller. At the microsecond level, the device interface simulates traditional channel units.

The adapters provide a limited network of connections between host processors and storage devices. For example (Fig. 4), two different processors can share a common tape controller as a convenient and simple mechanism for a long-line connection. They can also communicate with each other through the trunks. The adapters are capable of decoupling by means of buffers, multiplexing the trunks by transferring from one adapter buffer to another, and shared usage of a common unit. Contention between two adapters up to 1000 ft apart on a common trunk (the reverse of the previously mentioned contention of two trunks for one adapter) can arise if both units request the trunk within a "window" of 1.5 μs. If this occurs, neither adapter is likely to receive a response, or possibly both responses will contain checkword errors. Either way, the adapters wait for a prescribed interval of time, then try again. No two adapters have the same retry intervals, which are assigned on the basis of a priority scheme; therefore, contention between two adapters cannot occur on the retry.

Such mini-network adapters could be added to a conventional installation, but would quickly bog down in contention if more than a few paths were needed simultaneously. To avoid this difficulty, a higher level network control is needed. This, together with execution of file software for the site, is the task of the network control unit.

Network Control Unit

By experience, designers have found that executing this file management software calls for extensive processing capability. However, the network control unit—a special-purpose computer—is designed as much for path management and buffering of high-bandwidth block traffic as for conventional file management. They demand high input/output (I/O) performance, which traditionally would require a large-scale machine, because in the past almost all computers were designed with the I/O power approximately balanced with the computational power. In this respect, the network control unit departs from tradition: it is a high performance, small machine with "super I/O" facilities.

The network control unit (NCU) comprises a network processor, memory, up to eight trunk processors, and a trunk matrix (Fig. 5). The network processor is the controlling element of the NCU. This is a 16-bit processor that executes more than 3 million instructions/s. It has direct access to the memory, which cycles in 100 ns and has a capacity of up to 131,072 bytes.

In the maximum configuration, the eight trunk processors, which are slaves to the network processor, also have direct access to the memory. In this case, the memory is configured in eight interleaved phases, thereby allowing all eight trunk processors to have simultaneous access. However, they are limited to simple decision-making and fast transfers between memory and trunks. They are connected to the network through an 8 x 16 matrix, through which each of the eight trunk processors can select one of the 16 trunks for transmitting or receiving.

The network processor has a general register structure, emphasizing register-to-register operation in high performance subroutines. Instructions execute in 200-ns cycles; most require only one cycle.

Its instruction set includes memory operand, register operand, and I/O instructions rich in the ability to manipulate bits and execute logical operations. In this case, I/O refers to sense and control functions within the network control unit, since the NCU's real I/O is controlled by trunk processors.

A sophisticated subroutine entry-and-return system allows stacking of subroutines and rapid interrupt handling.

The NCU memory consists of eight independent banks, operating at 100 ns for a read/write cycle. It is made from a 1024-bit emitter-coupled logic chip, with access time of less than 60 ns. Every other cycle is given to the network processor. On the alternate cycles, all eight trunk processors are given access to the eight banks, each one to a given bank; during eight consecutive 200-ns periods, a trunk processor can have access to all eight banks. Because of this alternation, trunk processor references to memory do not affect the network processor. If a block transfer or a sequence of register-only instructions is being executed, the trunk processor will appear to run at the 200-ns rate, since the memory references are sequential; but with random references to memory, each trunk processor averages 800 ns/reference.

When one trunk processor executes one block transfer—its major function, it requires one random cycle of 800 ns at first; the transfer continues at 200 ns per 16-bit memory reference. Total transfer rate is 80 megabits/s—more than enough to keep the 50-megabit/s trunk busy. *All* trunk processors can perform simultaneously at this rate, netting a maximum trunk rate of 400 megabits/s (8 x 50). This in no way degrades performance of the network processor.

Through the trunk matrix hardware, each trunk processor can select any one of the 16 trunks. Two trunk processors may, in fact, use a trunk for fast block transfer, memory-to-memory. Like the network processor, the trunk processor also has a general register structure, with special emphasis on simple decision-making and block transfer. Principal role of the trunk processors is to multiplex data blocks efficiently on the coaxial network. Under certain conditions, a trunk processor may take over part of the function traditionally handled by the device controller; the network adapter can then be coupled directly to the device, eliminating the controller.

New Storage Technology

With the advent of new storage devices augmenting magnetic disc, the potential of an online storage hierarchy may be realized. For example, mass storage systems now being offered eliminate manual tape mounting and provide staging to discs. The possibility now exists that data will migrate within the hierarchy created by this new device, with the least used data residing on the least expensive media.

New solid-state technologies also can be conceived as another level in the hierarchy just above magnetic disc. Electron beam memories, bubble memories, and memories based on charge-coupled devices are candidates for this level. Even magnetic core storage could be used.

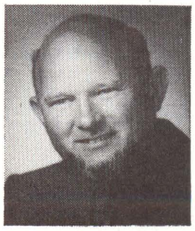
For data to migrate in such an environment of three different classes of technology, a sophisticated network is necessary. The network storage system is directed at this class of installation, allocating space, cataloging the files, and insuring the security of the whole system, no matter where the data may migrate.

Summary

Conventional CPUs and channels are considered architecturally inadequate to handle the projected future data traffic in a local site. However, a very high bandwidth serial network and a specially designed traffic management processor can outperform the conventional systems now in operation.

James E. Thornton, president of Network Systems Corp, has experience in the development of large scale computer systems. He holds a BS degree in electrical engineering from the University of Minnesota.

Gary S. Christensen, vice president/general manager of Network Systems Corp, holds a BS degree in electrical engineering from Iowa State University. He has participated in the development of communications and input/output systems products.



Peter D. Jones, vice president-development for Network Systems Corp, has experience in development of large computer systems software. He received a BS/MS degree in science and engineering and a PhD degree in aeronautical engineering from Sydney University, Australia.

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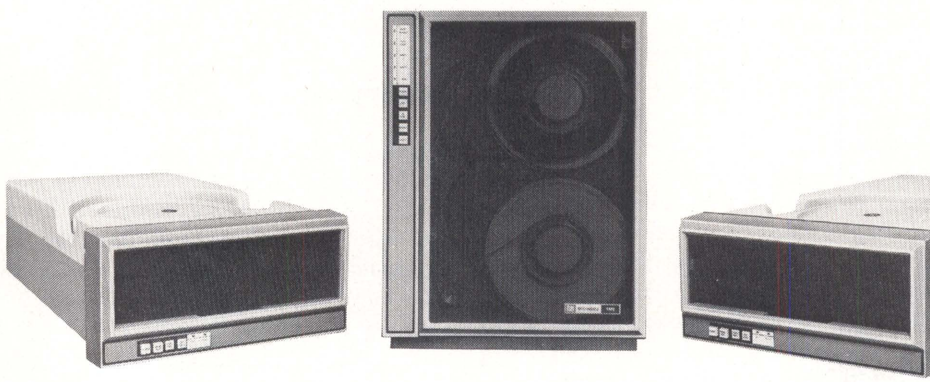

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Although microprocessors that form part of larger systems do not often require manual access, they should be designed to permit such access during debugging and maintenance

Operator's Console Considerations in Microprocessor System Design

Jeff Little and A. Thampy Thomas

Intersil, Incorporated
Cupertino, California

Certain architectural features must be provided in microprocessors to facilitate the use of a control panel. Although most microprocessor-based systems, when they reach the production stage, are integrated as subassemblies within larger systems, and thus rarely need their own control panels, a panel remains necessary for designing and debugging prototype systems, and for maintaining production-level systems. Minicomputer-based systems, on the other hand, normally come complete with dedicated control panels.

The operator's console or control panel in a computer system, whether micro-, mini-, or macro-, consists of an array of switches and indicators to simplify computer operation and permit maintenance (Fig. 1). Switches and indicators permit programmer or operator to start and stop program execution, examine and modify contents of main memory, select various modes of operation, and load and execute short machine-language programs.

In minicomputers, the internal registers and control lines are accessible, allowing the control panel to be directly and physically connected ("hardwired") to them. Through these connections, the panel sends logic signals that control the sequence of states in the minicomputer for the desired operation. Obviously, a hardwired control panel cannot be used with a microprocessor, because its register and transfer signals are not externally accessible. The alternative is to modify and display the internal data under program control.

Architectural features of a microprocessor that are required for control panel connection must include a means of communication between panel and micro-

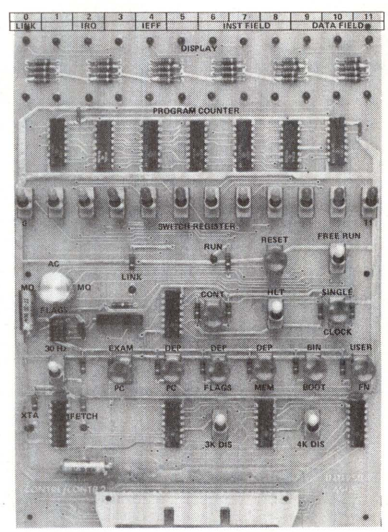


Fig. 1 Intersil 6100. Operator's console consists of a memory module, which plugs into the system bus and connects through a flat cable with this display module, carrying switches and indicators as shown

processor and a memory to store control panel routines that replace the hardwired connections. Since panel operation is inherently asynchronous, the processor must be interrupted to carry out panel operations. Through the interrupt system, an external event causes the central processor unit (CPU) to leave the current program segment, execute a predetermined service routine, which services the external request, and return to the original program. Interrupt capability may be enabled or disabled under program control. After the processor recognizes an interrupt request, the interrupt system is automatically disabled, so that no additional requests are acknowledged until it is re-enabled under program control.

However, the panel should not communicate with the processor through the normal interrupt channel. An interrupt is granted when the processor executes a hardwired subroutine call to the interrupt service routine. This call is usually built into the processor sequencer, requiring the entry point of the subroutine to be in a read-only location. Similarly, control panel routines should be stored in nonvolatile read-only memory (ROM) devices. However, the control-panel interrupt request line to the CPU is treated differently from other interrupt request lines, because the conventional interrupt system is inactive when the processor is halted; and even when it is running, the interrupt system may be disabled. Clearly, the panel-to-CPU communication link must permit the processor to recognize the console interrupt when it is halted, and allow it to go into run state to execute the panel routine. If the processor is not running before it receives the interrupt, it should return to that state when exiting the panel program.

"Transparent" Panel Memory

Panel routines require memory. If part of main memory is occupied by panel software, obviously that portion is not available to the user. For that reason, and because the final version of the system may not have a control panel, control panel memory should be distinct from main memory. This separation permits system designers to use all of main memory for the specific system application. It also permits a standalone portable panel to be designed, with the routines residing in panel memory—which, however, can share the same addressing space as the main program, so that console operations are transparent to system users.

Four Microprocessor Consoles

The microprogram of the National Semiconductor IMP-16 allows two kinds of interrupts—a normal and a high-priority interrupt (CPINT) from the control panel (Fig. 2). If the interrupt system is enabled, the processor services a peripheral device interrupt by executing a microprogram-controlled subroutine call to location 0001 in main memory; CPINT is serviced by jamming an externally hardwired instruction on the data lines, overriding anything else that may be there at the moment. Both this instruction and the one in 0001 cause a branch to the appropriate routine.

Characteristics of Four Microprocessors

The *National Semiconductor IMP-16* is a 16-bit microprocessor configured around the company's microprogrammable GPC/P devices, which are large p-channel MOS circuits comprising one control read-only memory (CROM) and four register-arithmetic-logic units (RALU). Each RALU processes four bits in parallel; the 16-bit unit is made up of four RALUs connected in parallel and controlled by the single CROM.

The *Intel 8080* is a single-chip, 8-bit parallel processor made in a high voltage n-channel MOS process. It is used with conventional standard read-only and read/write memories and other integrated circuits, which are assembled on one or more printed circuit boards to make a system.

The *Motorola 6800* microprocessing unit forms the nucleus of the company's 8-bit microprocessor family. It is implemented with a 5-V, n-channel MOS process. Its instructions range from one to three bytes in length; the programmer has access to two accumulators, one index register, a stack pointer, and a condition code register. Two-byte instructions operate on data in the first 256 memory locations; 3-byte instructions can get their data from anywhere in memory (maximum capacity 65,536 bytes). Input/output devices are connected to a unified bus in parallel with one another and with memory; their addresses are part of the memory address space.

Intersil's IM6100 is a 12-bit microprocessor made with silicon-gate CMOS technology on a single chip. Its architecture is compatible, both in software and in programmed input/output interface, with that of the PDP-8/E minicomputer of Digital Equipment Corp.

The processor's microprogram also provides a system power-on reset. When the reset is active, the processor executes an instruction sequence beginning at the next to last location in memory. In most applications, this sequence consists of initialization routines and other supervisory program segments. By keeping these segments in the top portion of memory, that portion can be ROM, and thus nonvolatile. Since the first 256 words are directly accessible from any part of memory with an 8-bit address, they should be implemented with

Fig. 2 IMP-16L. National Semiconductor Corp offers this prototyping system for use with its IMP-16 microprocessor. Control panel is both an operator's console and a programmer's panel

read/write memory (RWM). The power-on reset signal can originate from a control panel or from elsewhere in a system without a control panel; therefore, panel features need be used only when required.

The Intel 8080 has only one interrupt request line, used by both control panel (Fig. 3) and external devices. If the interrupt system is enabled, the CPU acknowledges an interrupt request by a return signal and then, during the next instruction-fetch cycle, inserts a 1-byte instruction on the data lines. This instruction is usually Restart, which forces a subroutine call to one of eight user-defined locations in the lower part of memory. The Restart instruction is externally hardwired. If the interrupt system is disabled under program control, no interrupt, whether external or from the control panel, will be acknowledged.

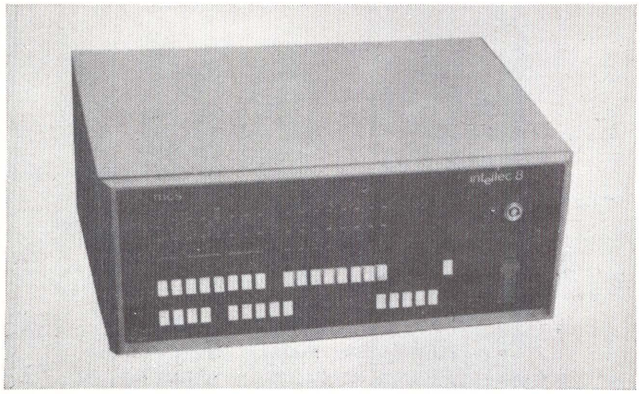


Fig. 3 Intellec 8. Offered by Intel Corp, this is a development unit for the company's 8008 microprocessor. Panel includes address, program sequence, and mode control switches, including a mode for programming p/ROMs

A system based on this processor can be initialized or halted even without a full panel. When system reset is active, the processor branches to memory location 0000, which contains the start of supervisory routines similar to those located at the top end of IMP-16 memory. This makes it necessary to implement lower 8080 memory locations with ROM. However, this is not a drawback, because 8080 architecture does not use paged memory references; every instruction that refers to memory must specify a full 16-bit operand address. No advantage is attained by implementing lower memory locations or particular segments as RWM.

The Motorola 6800 has two interrupt request lines: IRQ, the conventional interrupt request line, which may be masked off under program control, and NMI, which is nonmaskable and may be used for the control panel request. The control panel, like many other peripheral devices, communicates with the microprocessor through a peripheral interface adapter (PIA) and a unified bus (Fig. 4). For the processor to recognize IRQ, its interrupt system must be enabled and the processor must not be halted.

The processor responds to an IRQ by executing a subroutine call indirectly through location n — 6, where n often is, but need not be, the highest memory location. Vector address pointers are at n — 2 and n for NMI and system RESET, respectively. Higher memory locations, containing the application program, are usually ROM; lower locations are RWM, accessible with paged memory references.

Thus, significant differences exist in the way these three microprocessors work with control panels. In summary, in the IMP-16 and the 8080, an instruction must be hardwired externally for the processor to recognize when it responds to a control panel interrupt. This hardwiring requires additional logic. On the other hand, the 6800 has a vectored control panel interrupt. Meanwhile, both IMP-16 and 6800—but not the 8080—can isolate panel requests from normal interrupts. In all three units, part of main memory must be disabled by logic that is built into the control panel, effectively replacing that portion with control panel memory, making the latter transparent to the user; the logic must also selectively re-enable parts of disabled memory so that it can be examined and modified during debugging.

The amount of external hardware required to do this depends on the amount of main memory needed in the application. If the user's program does not fill the entire addressing space, the additional hardware requirement may be insignificant. Few microprocessor applications require 65,000 bytes of memory. However, in minimum systems, the few words actually needed may be scattered throughout a large area of addressing space, to reduce the amount of external logic that full decoding would require.

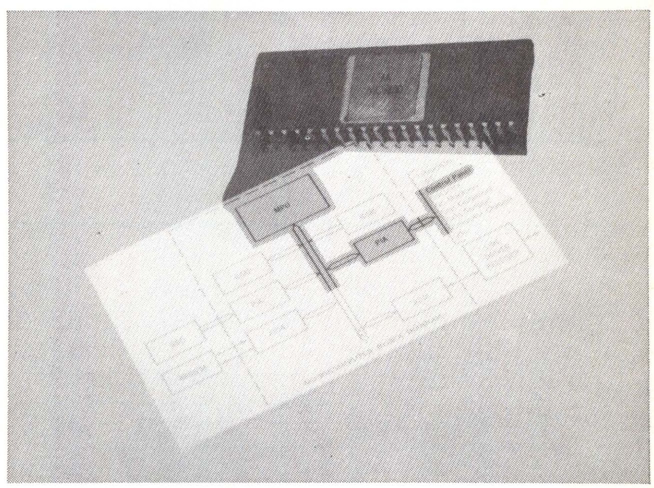


Fig. 4 Just another peripheral. Motorola 6800 microprocessor uses a unified bus for all its peripheral devices, one of which is the control panel

For example, memory for the 6800 is usually assembled from 128 x 8 RWM chips and 1024 x 8 ROM chips; a minimum system consists of one of each of these and the microprocessor itself. However, the microprocessor still addresses this very small memory with a 16-bit address. Larger memories are packaged on up to four printed circuit boards, each having 16,384 words; the two most-significant address bits point to one of the four boards (Fig. 5). In conventionally addressed minimum systems, both bits would be 0.

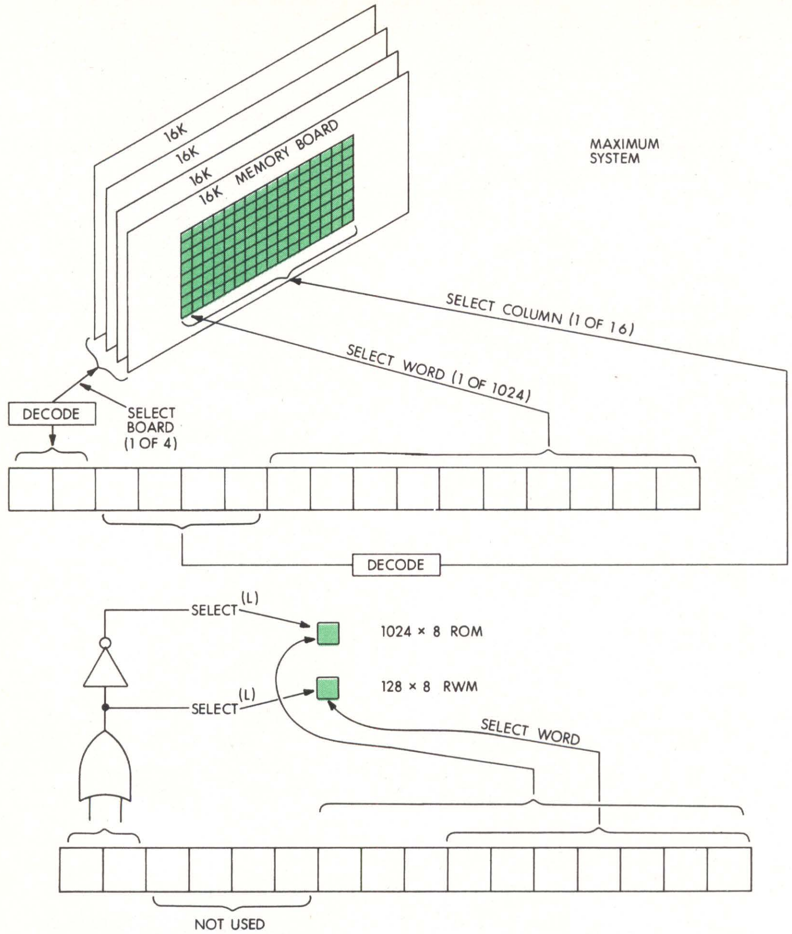
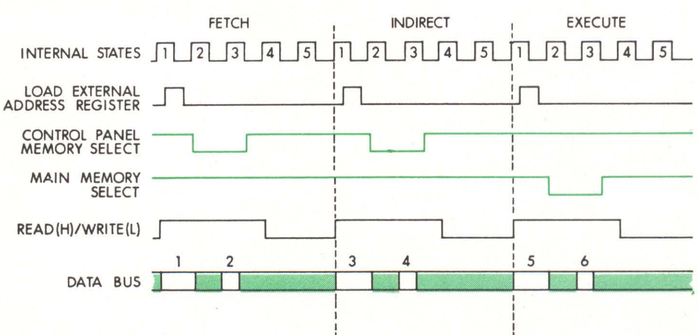


Fig. 5 Big address, little memory. External hardware can sometimes be reduced by addressing a small memory as if its contents were scattered throughout a large one. Word-select bits are decoded within memory chip



(a)

```
/IM6100 CONTROL PANEL PROGRAM TO EXAMINE THE
/CONTENTS OF A MEMORY LOCATION IDENTIFIED
/IN THE PANEL SWITCH REGISTER

EXAM, CLA OSR      /CLEAR ACCUMULATOR AND READ SWITCH REGISTER INTO IT
      DCA POINTER  /DEPOSIT THE AC IN MEMORY LOCATION POINTER AND CLEAR AC
      TAD I POINTER /GET FROM MAIN MEMORY THE CONTENTS OF LOCATION
                   /INDICATED BY THE CONTENTS OF POINTER, PUT
                   /IT IN THE AC, AND DISPLAY THE AC
```

(b)

Fig. 6 Displaying main memory. With indirect addressing, contents of any main memory location can be displayed or altered. Timing chart shows how panel memory and main memory are alternately selected. Data bus shows (1) instruction address, (2) instruction from panel memory, (3) indirect address, (4) operand address from panel memory, (5) operand address, and finally (6) the operand itself from main memory. Three-instruction sequence first clears accumulator and puts the contents of switch register into it; then deposits this number in the memory location named POINTER, clears the accumulator again, and finally reloads it from the main memory location indicated by the contents of POINTER (originally set manually in switch register) and displays it on the operator's panel. The last instruction has an indirect address

To avoid external decoders, the 10 least-significant bits can address the ROM in the usual way, while the seven least-significant bits address the RWM; if the high-order bits are 00, RWM is addressed, and if either or both are 1, ROM is addressed. Bits 11 through 14 are not used. Thus, the whole 65,000-plus address space is used to select a maximum of 1152 words.

The IM6100 (Intersil, Inc) requires a transparent control panel to retain its built-in compatibility with the PDP-8, which has a hardwired console and thus uses no main memory for panel functions. This microprocessor has two interrupt request lines: interrupt request (INTREQ) and control panel request (CPREQ). The processor responds to either interrupt by depositing the contents of the program counter in memory location 0000, and beginning execution of the interrupt service routine.

The processor responds to INTREQ only if the interrupt system is enabled and the processor is running; program counter contents go to main memory. The interrupt system is disabled while the processor executes the interrupt service routine, which begins at location 0001. On the other hand, CPREQ is acknowledged whether the processor is running or halted; if the latter, it is put temporarily into the run state to execute the panel routine, then reverts to its original state. Program counter contents go to the panel memory, and the interrupt service routine begins at location 7777 (octal notation), which contains a jump instruction to the routine's actual starting point. This and nearby locations at the top end of the memory are ROM. CPREQ is also independent of the main interrupt enable; however, an interrupt flag called CNTRL FF is set when CPREQ is acknowledged, to prevent further panel requests from being recognized.

This processor communicates with main memory by activating the memory select (MEMSEL) line, which is the chip-select line for the individual ICs. As long as CNTRL FF is set, CPSEL becomes active instead of MEMSEL to communicate with panel memory.

Although panel memory is completely separate from main memory, every main-memory location is accessible to panel memory—for example, to permit the computer operator to examine the contents of a specific main memory location. Access utilizes indirect addressing, in which the address code of an instruction refers to a memory location containing the address of the desired operand (Fig. 6). (A direct address is that of the operand itself, omitting the intermediate step.) Both instruction and indirect address are in panel memory; however, the effective address (which is obtained from a bank of manual switches on the panel, set previously to the address the operator wants to examine) points to a main-memory location.

In the same way, an indirect store instruction enables a main-memory location to be modified.

While the processor is in panel mode, all but one of the instructions that modify the normal interrupt system are disabled. The exception is Interrupt On, which re-enables the interrupt system following the routine that services a normal interrupt. When the processor is in panel mode, Interrupt On resets CNTRL FF after executing the next sequential instruction. If that instruction is an indirect jump through 0000, the processor thereby exits from panel mode. That location contains either the return address stored there by CPREQ, or a new starting address placed by the operator during the panel routine.

Some panel functions cannot be easily programmed. An example is Single Instruction capability, which permits the processor to execute one instruction, when the operator presses the start button, then stops it. It is a rather primitive means of debugging programs. In the IM6100, this function and the similar single-clock functions are built into the chip, as are Halt, Continue, and Initialize. These functions permit a minimum system to be controlled without an external panel.

All functions of the PDP-8/E console can be implemented using only eight words of RWM and 64 words of ROM.

Conclusion

The IM6100 serves as an example of how microprocessor design can facilitate panel functions. Although there are various other ways of implementing these same features, the IM6100 approach is simple and straightforward. It requires only two additional pins—for CPREQ and CPSEL lines—and one additional line in the internal programmed logic array, which controls the sequence of microprocessor applications. The approach does not require any new instructions and does not change the processor state.

Several panel options can further increase the usefulness and flexibility of a microprocessor-based system. For example, the panel can be used as a maintenance tool if test and exercise programs are stored in panel memory. The memory can also store bootstrap loaders that are transparent to main memory. Each additional feature can be implemented by a small routine in software, requiring only a slightly larger panel memory.

This design approach makes the microprocessor panel appear to be a completely independent standalone device that can be plugged into a socket on the processor board whenever console functions are needed, and unplugged afterward without disturbing any part of the user system.

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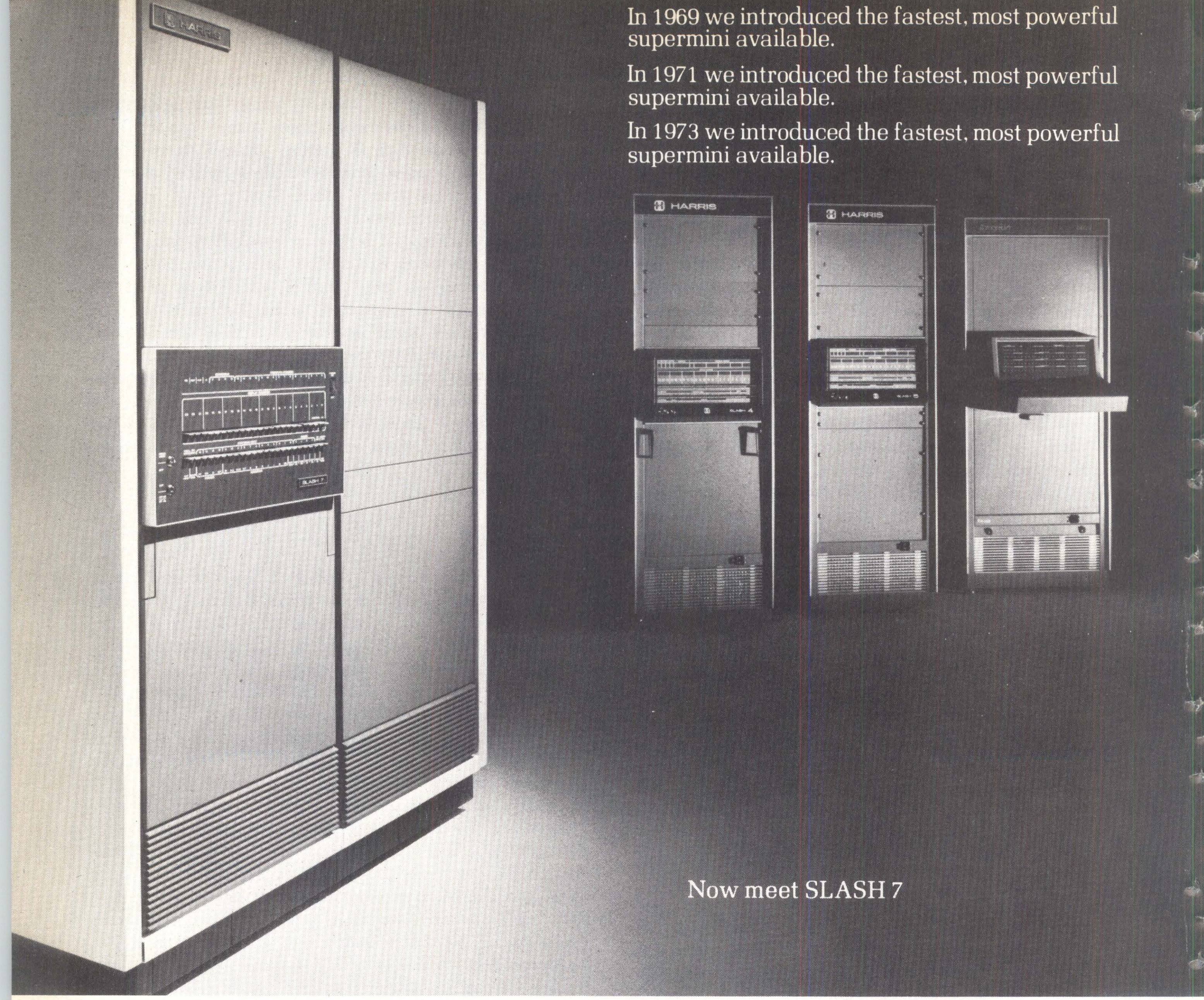

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CIRCLE 45 ON INQUIRY CARD

Cyclic redundancy codes expressed in purely mathematical terms may be precisely stated, but are not necessarily easily understood. For engineers who may be using IC implementations of these codes, but who lack real understanding of how the circuits work, this article presents the fundamentals of CRC operation and implementation

Understanding Cyclic Redundancy Codes

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When dealing with sophisticated error-correcting codes, designers sometimes get the uneasy feeling that they don't quite know what's going on in the equipment for which they are responsible—particularly now that cyclic redundancy codes are being used more and more, especially in newer disc and tape systems and in data transmission. These applications may fall short of their full potential if their designers, responsible for implementing these codes in large-scale integrated circuits, don't have insight into the actual working of the code.

The codes are not really difficult. Although they are often described in mathematical terms, their operation and implementation are reasonably straightforward. An understanding of the codes, based on a minimal mathematical background, will lead directly to practical insight.

Basic Theory

Coding theory treats data mathematically in polynomial form.[1,2] Since polynomials can be tricky to think about, a mental image of a data polynomial is essential.

A polynomial is a summation of various powers of one or more variables, with a coefficient attached to each term in the summation—for example,

$$ax^2 + bx + c$$

In this cyclic code application, all coefficients are binary and there is only one variable. This binary variable, usually represented by x, is present only to permit mathematical treatment; coefficients are the real data. Each bit in a data string is assigned as coefficient to a unique power of x; the powers may be thought of as separators or weights of the bits in a string. As many powers of x are used as are needed for data bits in the string. In the simplest case, the highest power of x is attached to the most-significant bit, while descending powers go in order with bits of lesser significance. (Sometimes, as described later, the highest power of x is attached to the least-significant bit.) For example, the string 10011011 can be represented as a polynomial, with the left-most element of the string the most significant:

$$x^7 + x^4 + x^3 + x + 1$$

The power of x attached to the least-significant bit is 0; thus, since $x^0 = 1$, the least-significant bit in the string stands without an attached variable.

Polynomials can be algebraically manipulated if their coefficients' arithmetic is understood. They are members of a modular number system—that is, all the ordinary integers, of whatever magnitude or sign, are mapped into a finite set of m integers, m being a positive integer called the modulus. Mapping is a representation of any integer, n, as the remainder resulting from division of n by m, or equivalently

$$n = i + km$$

where k is any integer. Thus, two numbers are said to be congruent modulo m if they leave the same remainders when divided by m. For a given m, all integers can be mapped into the finite set of integers,

$$
\begin{array}{r|l}
 & x^3 + x + 1 \\
\hline
x^5 + x^3 + x + 1 & x^8 + x^5 + x^2 + 1 \\
 & x^8 + x^6 + x^4 + x^3 \\
\hline
 & x^6 + x^5 + x^4 + x^3 + x^2 \\
 & x^6 + x^4 + x^2 + x \\
\hline
 & x^5 + x^3 + x + 1 \\
 & x^5 + x^3 + x + 1 \\
\hline
 & 0 = R(x)
\end{array}
$$

(a) $D_a(x) = (x^3 + x + 1)(x^5 + x^3 + x + 1)$
$= Q(x)G(x)$

$$
\begin{array}{r|l}
 & x^2 + 1 \\
\hline
x^5 + x^3 + x + 1 & x^7 + x^3 + 1 \\
 & x^7 + x^5 + x^3 + x^2 \\
\hline
 & x^5 + x^2 + 1 \\
 & x^5 + x^3 + x + 1 \\
\hline
 & x^3 + x^2 + x = R(x)
\end{array}
$$

(b) $D_b(x) = (x^2 + 1)(x^5 + x^3 + x + 1) + (x^3 + x^2 + x)$
$= Q(x)G(x) + R(x)$

Fig. 1 Division of two polynomials. Division has two possible results, where $R(x) = 0$ (a) and where $R(x) = 0$ (b). Both are shown in ordinary algebraic notation. The coefficients are added modulo 2, which means addition and subtraction are the same. There is no borrow or carry with this modular arithmetic

0 to $(m - 1)$ inclusive. For example, if $m = 7$, then $n = 57 = 1 + 8 \cdot 7$; $k = 8$, $i = 1$, and $57 \equiv 1 \bmod 7$. Likewise, if $m = 7$, then $n = -33 = 2 + (-5) \cdot 7$; $k = -5$, $i = 2$, and $-33 \equiv 2 \bmod 7$.

In any modular system, given two congruent numbers and any other integer, the sums, differences, and products of those numbers and that integer are also congruent; mathematically, for any x, if $a \equiv b$,

$$a + x \equiv b + x, \quad a - x \equiv b - x, \text{ and } ax \equiv bx$$

Furthermore, if and only if the modulus is prime, a common factor can be cancelled in two congruent numbers without destroying the congruence; that is

$$ca \equiv cb \quad \text{implies} \quad a \equiv b$$

In particular, for $m = 2$, the binary case, all numbers are mapped into either 0 or 1. Since -1 is mapped into $+1$, addition and subtraction operations are identical—a fact that underlies all basic manipulations of binary cyclic codes.

Division of one polynomial, $D(x)$, by another, $G(x)$ (Fig. 1), produces a quotient polynomial, $Q(x)$, and usually a remainder polynomial, $R(x)$, if the division is not exact:

$$\frac{D(x)}{G(x)} = Q(x) + \frac{R(x)}{G(x)} \quad \text{or}$$

$$D(x) = Q(x)G(x) + R(x)$$

A basic coding concept is to modify a polynomial that represents a string of data so that it is exactly divisible by another polynomial; the divisor is called the generator polynomial $G(x)$. This modification is done by appending certain calculable bits, called redundancy bits, to the data string; these extra bits are essential in any error detecting and correcting code, because they distinguish code words containing errors from other code words.

Redundancy bits are determined by dividing the data polynomial by the generator polynomial and adding the resulting remainder to the original data polynomial. Since, in the modulo-2 (binary) arithmetic system, the sum and difference are the same, adding the remainder to the data is equivalent to subtracting it. In the second of the two equations demonstrating polynomial division, when the remainder is subtracted from both sides, the right side becomes a product of polynomials:

$$D(x) - R(x) = Q(x)G(x)$$

This product is clearly divisible by $G(x)$, since that is one of its factors. Therefore, the division and addition forms a new polynomial that is always exactly divisible by $G(x)$. Such polynomials correspond to code words; the remainder comprises the redundancy bits.

If the complete polynomial code word to be transmitted or stored is designated $C(x)$, then

$$C(x) = D(x) + R(x) = Q(x)G(x)$$

When data with redundancy bits attached, $T(x)$, are received or fetched, they may be divided again by $G(x)$. If the remainder is 0, all bits are assumed to have arrived unaltered. (Conceivably, the error could be such that the disturbed polynomial is still divisible by $G(x)$. This disturbance would constitute an undetectable error.)

Any disturbances in the received polynomial can be represented by an error polynomial, $E(x)$. When $E(x)$ is subtracted from the received polynomial, $Z(x)$, or equivalently added to it, the result is the sum of the correct data and redundancy polynomials:

$$T(x) = Z(x) - E(x) = Z(x) + E(x)$$

Obviously, any attempt at error correction requires that this error polynomial be found.

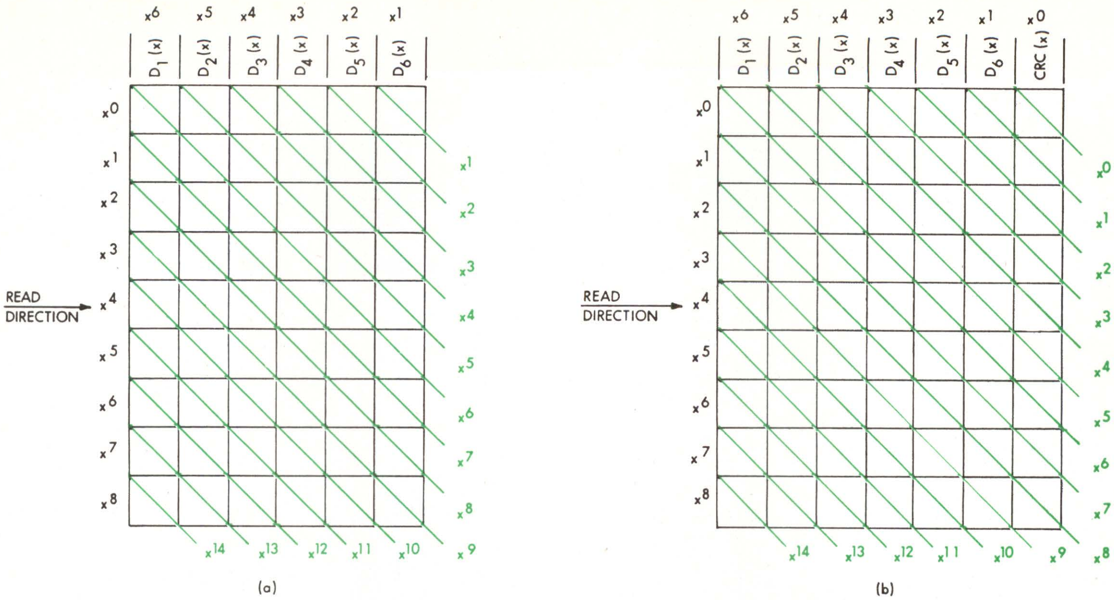


Fig. 2 Data as written on tape. Data form an array (a) with successive powers of x from 1 to the highest (here 14) lying along the diagonals. When the CRC character is added (b), the full set of powers of x from 0 up is included. They are properly arranged so that data which arrive first occupy the higher powers of the net polynomial. Black squares represent bit locations in error (see text)

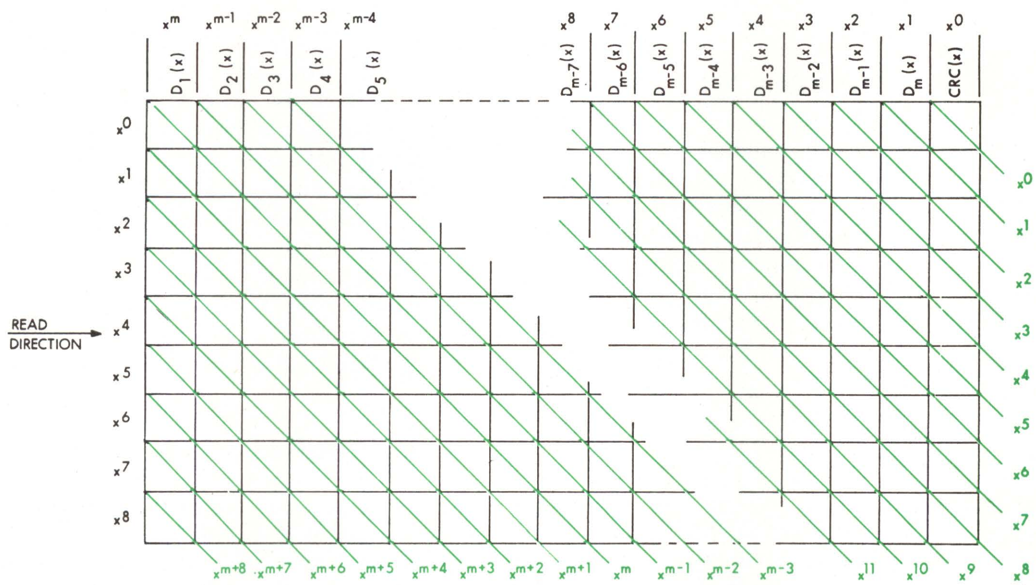


Fig. 3 Long tape record. A record of m data characters would appear on the tape as a lengthened array. Its increased length would only increase the highest power of x in the net polynomial. Visualizing the extension of the net polynomial by adding data is important

CRC Polynomial Structure

In the 9-track cyclic redundancy check (CRC) code defined in the standard for 800-bit/in. magnetic tape, issued by the American National Standards Institute, a ninth-degree generator polynomial is specified:

$$G(x) = x^9 + x^6 + x^5 + x^4 + x^3 + 1$$

Any remainder after division is of degree eight or less, corresponding to a 9-bit data word, which is the format of the tape system.

The standard includes a rather formidable polynomial for the CRC character itself. Data consist of a sequence of 8-bit bytes plus parity; these bytes contribute to formation of a net polynomial:

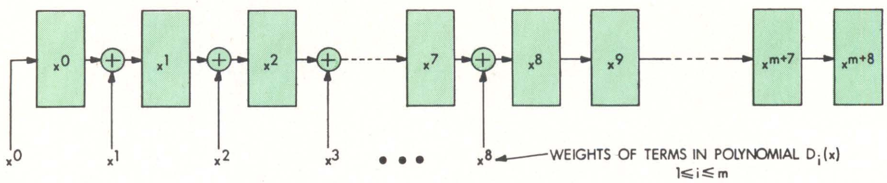
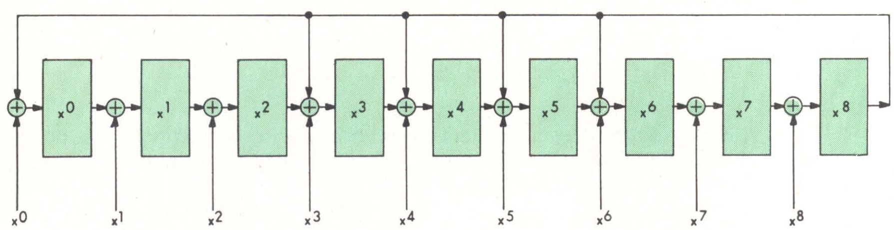


Fig. 4 Hypothetical net polynomial formation. Potential net polynomials are accumulated in a parallel-load serial shift register. Shifting the data right effectively multiplies them by x. Parallel loading into the low-order places automatically enters a data polynomial in correct relationship to previous entries if a right shift occurs after each parallel load

Fig. 5 Practical net polynomial formation. Division by the generator polynomial is accomplished when a shift that would create x^9 is fed back to its equivalent terms of lower order instead of passing on into a continuous register. In so doing, the growing net polynomial is continuously reduced in a division-like process. The circuit is then a polynomial division circuit for a fixed divisor



$$x^mD_1(x) + x^{m-1}D_2(x) + \ldots + xD_m(x) = \sum_{i=1}^{m} x^{m+1-i}D_i(x)$$

Since each 9-bit byte is itself a data polynomial, the net polynomial is a summation of data polynomials after each is multiplied by a power of x. This power is the number of the particular polynomial, attained by counting backward from the end of data as recorded.

The CRC character is the remainder after dividing the net polynomial by the generator polynomial and, as such, is congruent to the net polynomial. This remainder is often given as

$$CRC(x) = \left[\sum_{i=1}^{m} x^{m+1-i}D_i(x)\right] \bmod G(x)$$

To illustrate the mathematical process, consider a short record of six characters [Fig. 2(a)]. Each track corresponds to a specific power of x in individual data polynomials, $D_i(x)$; the powers are listed along the left edge of the array. (Assignments are shown ascending according to track number; although this does not correspond to the standard, assignment is not important in understanding code operation.) Along the top edge of the array are the powers of x, which multiply each data polynomial (the columns) to produce the net polynomial:

$$x^6D_1(x) + x^5D_2(x) + x^4D_3(x) + x^3D_4(x) + x^2D_5(x) + xD_6(x)$$

Maximum degree of this polynomial is 14, which occurs when the most-significant bit of $D_1(x)$ is 1, so that $D_1(x)$ contains the term x^8. The term x^{14} in the net polynomial results from multiplication of this term by x^6. All lower powers, except x, in the net polynomial are the sum of several coefficients, formed by adding the data bits modulo 2 along each diagonal. In longer records of length m, the maximum degree of the net polynomial is $(m + 8)$ (Fig. 3).

The CRC character for any net polynomial is calculated through division by $G(x)$, as described previously; the 9-bit remainder is written on the tape like any other data character. This adds another column to the array [Fig. 2(b)], and an extra bit in the diagonal summation, which corresponds to the power x^0. Now the net polynomial potentially contains all powers of x from 0 through $(m + 8)$.

Implementation

Circuits to perform the division are either available in chip form or may be implemented from standard logic components. All such circuits follow the same basic principle, to produce the remainder after division by $G(x)$. Anything exactly divisible by $G(x)$ is congruent to 0; $G(x)$, of course, is exactly divisible by itself, and so is congruent to 0. Thus, set $G(x) = 0$ and solve for x^9:

$$x^9 = x^6 + x^5 + x^4 + x^3 + 1$$

Then, whenever x^9 occurs, it may be replaced by all lower-order terms of the generator polynomial.

In a long register of $(m + 9)$ elements, each element represents a memory for the coefficient for one power of x (Fig. 4). If all elements are set to 0, and a 9-bit data polynomial is loaded into the first nine positions and shifted right, each shift multiplies the polynomial by x. If the shift register is $(m + 9)$ bits long, parallel loading of successive data polynomials followed by a right shift forms the entire net polynomial. Successive characters are added modulo 2, which in logic is simply an exclusive-OR.

Successive characters, arriving as ordered in the record, are shifted $(m + 1 - i)$ times. This means that higher powers are created by early data, in accordance with Fig. 2.

For each bit that overflows from the x^8 position, a feedback substitution of congruent terms for x^9 can be made (Fig. 5). Overflow from x^8 may occur with every shift after the first. This enables the register to have only nine elements; the remainder of the division process is found in the register after all characters have been loaded. It is transmitted or stored as the last character of the record. If feeding back output of the x^8-register position is puzzling, remember that shifting is equivalent to multiplication by x; for a bit to enter the feedback loop, a shift is required, transforming x^8 into x^9. Configurations[3] other than that shown in Fig. 5 may produce desirable properties, such as speed.

Lowest-order term of the net polynomial is x^1, whereas when all data have been entered, the arrangement of Fig. 4 will have an entry in x^0. This can be corrected in either of two ways: (a) by simply shifting the data once more, with no input after the last entry is made; or (b) by premultiplying all bits by x. Premultiplication is done by entering all bits one position to the right of their locations in the diagram. This alternative requires that an exclusive-OR be located at the output of x^8 rather than at the input of x^0, which now receives only feedback.

Using CRC in Recovery

On recovery of data from a transmission channel or from storage, an identical circuit is used, because division by $G(x)$ is still central. If, after division, the remainder is not 0, an error has been detected; it may or may not be correctable. Although theorems dealing with correctability are beyond this presentation, it is not difficult to see how this code corrects one track in error.

An error polynomial, $E(x)$, is associated with the track in error, corresponding to a row rather than a column of Fig. 2. Its bit separators or weights are, therefore, the values of column weights listed at the top edge of the array. They run downward from m to 0 in the forward direction. For example, suppose the black squares in Fig. 2(b) represent bit locations in error. The corresponding error polynomial is $E(x) = x^6 + x^4 + x^3 + 1$. Formation of the net polynomial is irrelevant whether as a sum of products over rows or a sum of products over columns; either way, the received information is the net polynomial plus its redundancy bits, plus the error:

$$D_{net}(x) + [D_{net}(x)] \bmod G(x) + x^tE(x) =$$
$$D_{net}(x) + R(x) + x^tE(x) =$$
$$Q(x)\ G(x) + x^tE(x)$$

Each term in the sum may be divided separately and the quotients added; but, since only remainders are of interest,

$$[Q(x)\ G(x)] \bmod G(x) + [x^tE(x)] \bmod G(x) =$$
$$0 + [x^tE(x)] \bmod G(x)$$

When the whole sum is run through a divider circuit, the result is $[x^tE(x)] \bmod G(x)$—a mapping of the error, multiplied by x to a power associated with the track on which the error occurs. In the example,

$$x^tE(x) = x^4E(x) = x^4(x^6 + x^4 + x^3 + 1)$$

To this point, neither the track nor the characters containing errors have been identified. To do this, perform a vertical redundancy check (VRC); that is, check for odd parity in individual characters across all nine rows. Characters without errors produce a VRC = 0; if only one row has an error, VRC = 1 for the corresponding characters. Weighted sum of all VRCs is $E(x)$. As data are recovered, the VRC is entered serially into the x^0 input of a pattern register, which is a division register similar to that used for the net polynomial, producing an error mapping or pattern, this time without the multiplication by a power of x.

Clearly, when only one track has an error, both division circuits contain the remainder of the same error polynomial; however, one is multiplied by the power of x that corresponds to the particular track in error. To determine that track, shift the pattern register to the right with no input, comparing each time with the contents of the CRC register. After t shifts, the two registers will match; the number of shifts identifies the track.

This operation may also be implemented so that the CRC register is shifted instead of the pattern register. For example, the division circuit receiving VRC can be adjusted so that $E(x)$ is premultiplied by x^9. To do this, enter the serial VRC data summed with the output of the x^8 flip-flop into the feedback path. Since 9 is always greater than t, the CRC register must be shifted with no input. Then, the number of shifts required to obtain a match is the count of tracks up from the bottom rather than down from the top.

Many patterns of multiple track errors will go undetected in the CRC alone. For example, any even number of errors along a diagonal will not affect the net polynomial. This situation will not, however, escape the attention of the VRC. Thus, to detect erroneous data, both CRC and VRC must be used; to be passed as correct, both checks must yield 0 for the data under examination. Unfortunately, some rare error patterns elude even this scrutiny.

Other Forms of CRC

Cyclic codes have many interesting properties. For example, the reciprocal of a degree-m polynomial $G(x)$ is $x^m\ G(1/x)$, which is the previously mentioned case of the powers of x in reversed order. In the code generated by $G(x)$, all code words, $C(x)$, which may be long records on tape, may be inverted. This is easily done by forming new words with the highest power of x attached to the least-significant bit. Mathematically this replaces each term x^k according to the relation $x^nC(1/x)$, where n is the maximum degree of a code word, $(m + 8)$ in this case. The set of words thus formed, $C^*(x)$, is also a code, with $G^*(x)$, the reciprocal of $G(x)$, as its generator.

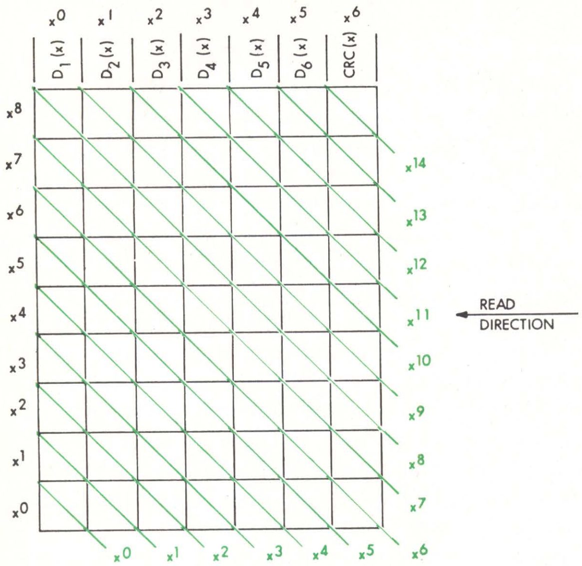


Fig. 6 Reading tape backward. Reverse read is not difficult because the array yields a reverse order of significance in the powers of x, by reversing the order of track assignments, as listed on the left edge. The powers given at the top of the array reverse automatically with the direction of reading. Essentially, the first data polynomial is now treated as a CRC polynomial. All that proper recovery requires is a division circuit that implements the reciprocal of the generator used in the forward direction

This property permits a record to be read backward, rather than requiring that the record be rewound for another forward run. To read backward, definitions of the powers of x in the original array [Fig. 2(a)] must be rearranged as shown in Fig. 6, even though recorded data are the same. As the read head passes over the tape in the reverse direction, it encounters 9-bit data words in the opposite order. According to the concept of code-word inversion, if powers of x on the net polynomial can be redefined properly, the code still works. Only the generator polynomial for recovery must be changed.

Reading backward automatically reverses the premultiplication terms listed along the upper edge, so that they decrease from right to left instead of from left to right. Values of individual bits of a data word must be reversed, to obtain desired weights for the net polynomial, shown at the ends of the diagonals. This is done simply in hardware by swapping data-read lines into the shift register before reading in reverse.

Two types of generator polynomials, often referred to as symmetric and asymmetric, are actually self-reciprocal and non-self-reciprocal, respectively. A self-reciprocal polynomial is its own reciprocal and, therefore, possesses symmetry. For example,

$$G(x) = x^8 + x^6 + x^2 + 1$$

is symmetrical, a fact that becomes more evident when the polynomial is written as a string of bits: 101000101. Reversing the order of these bits, which is equivalent to forming the reciprocal of the polynomial, produces a new string that is indistinguishable from the old. In contrast, the reciprocal of an asymmetrical polynomial is a new polynomial. As a generator, the reciprocal polynomial remains the basis of a code on the same data; the only change is the feedback configuration of the shift register circuit.

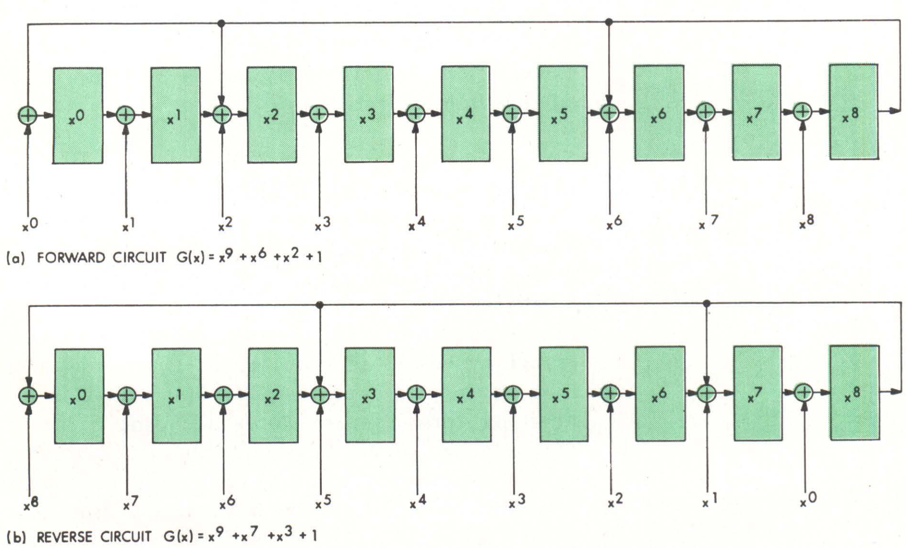


Fig. 7 An asymmetric generator. The auxiliary CRC code in the new 6250-bit/in. tape recording method is a good example of asymmetric polynomial codes. Input bit-weight assignments are relative to the forward direction; the input configuration is reversed in the reverse read circuit exactly as it is with symmetric CRC. The only difference is in the feedback, because the polynomial used in the reverse direction (b) is the reciprocal of that in the forward direction (a), and because the polynomial is asymmetric, and therefore not its own reciprocal

This feedback is the correlation between generator polynomial and circuit. It implements the division. By changing the feedback, the generator polynomial is altered. As a result, if the generator polynomial is self-reciprocal, reverse read requires no change in feedback, only data-line swapping—whereas if the generator is non-self-reciprocal, both feedback and data lines must be altered.

Until recently, most systems used the symmetrical approach, since its forward and reverse shift register hardware are identical. However, development of high density tape systems has produced applications for codes generated by asymmetric polynomials. An example is the forward and reverse shift register circuits (Fig. 7) that implement one of the generator polynomials in the proposed standard for recording at 6250 bits/in., now before the American National Standards Institute (ANSI).

The advantage of asymmetric codes is not immediately obvious. If more coding power is required as a check against undetectable errors, which elude the chosen polynomial, using additional symmetric codes might seem more straightforward. However, a deeper look into error code properties reveals the value of asymmetry. Further mathematical insight is necessary to uncover all details, but one relatively simple property is called cycle length, which can be defined as the number of shifts necessary in a feedback register after a specific bit pattern (such as a single 1) has been loaded, to restore that pattern. For an n-element register, cycle length is never more than $2^n - 1$; for some feedback combinations, it is much less. This property helps indicate a code's response to certain arrangements of errors. Codes of short cycle length are more susceptible to failure with short error sequences than those having long cycle lengths. Symmetric codes, in general, have short cycle lengths, while asymmetric codes have long cycle lengths. To obtain a broader range of checking ability, both types of codes should be applied to the data. This is the case, for example, in the proposed ANSI standard. The asymmetric generator from that standard (Fig. 7) is referred to as an auxiliary CRC code primarily because it is used with a symmetric CRC (a carryover from the older 800-bit/in. standard) against errors that are undetectable or uncorrectable by the symmetric code alone. Both regular and auxiliary CRC codes in the proposed standard apply to data blocks that may include many thousands of characters. A third cyclic code, also specified in the standard, covers groups of seven characters; its generator is also symmetric.

Both symmetric and asymmetric generator polynomials usually have $(x + 1)$ as a factor. For example, a previously cited CRC polynomial may be written

$$\begin{aligned} G(x) &= x^9 + x^6 + x^5 + x^4 + x^3 + 1 \\ &= (x + 1)(x^8 + x^7 + x^6 + x^4 + x^2 + 1) \end{aligned}$$

This $(x + 1)$ factor insures even parity over the entire code word, net polynomial plus redundancy.

Because all code words are divisible by $G(x)$, they are also divisible by any factor of $G(x)$. This makes $(x + 1)$ another generator polynomial that represents feedback around a single flip-flop that counts, modulo 2, the number of 1's present in a net polynomial. If the count is odd, then the result in the flip-flop is 1; when added to the record, this result makes overall parity even. However, if an even number of 1's are present, the result in the flip-flop is 0 and the parity remains even.

Thus, when the CRC character is added, the record contains an even number of 1 bits. Using this information, from the number of data words recorded, the parity of the CRC character can be predicted. Since all bytes individually have odd parity, an odd number of them have cumulative odd parity. Therefore, since the total record must have even parity, the CRC character must have odd parity. Similarly, an even number of data bytes requires an even-parity CRC character. In some realizations, the CRC character written on the tape has an odd number of inverted bits. This, of course, alters the parity of the written CRC and of the total record, making the latter odd parity and the CRC character the opposite of that described previously. This is done in systems where the CRC character is followed by a longitudinal redundancy check (LRC) character, which is an even-parity check on individual tracks the full length of the record. The inversion assures that the LRC character has odd vertical parity—a desirable trait, because it matches the parity of individual data bytes, and permits a check on the LRC character during recovery.

Some of the errors that have been described as especially difficult to detect are revealed with an LRC similar to the VRC. Correct data also produce LRC = 0.

Conclusion

Pioneers in the development of error-correcting codes worked without the aid of mathematics that exists today. They depended on insight into patterns and on the meager digital hardware available at that time. Today, error-correcting codes are, indeed, sophisticated mathematical ideas put into use in digital systems. However, they need not be a black magic box, as some users view them. While original research in coding may be left, for the most part, to modern algebraists, understanding what has been and what can be implemented is within the grasp of most digital engineers.

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Robert Swanson, currently completing his PhD degree in electrical engineering at the University of Arizona, is researching the use of hardware design languages in computer and logic design. His experience includes disc and tape error correction codes and microcomputer designs.

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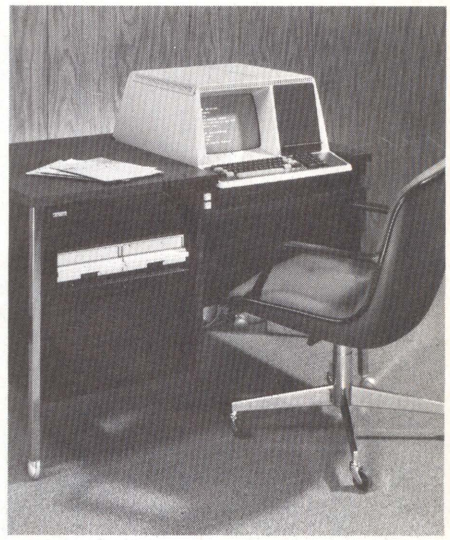

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DESIGN NOTE

Expanding a Memory Without Plug-Compatibility

Charles E. Cohn

Argonne National Laboratory
Argonne, Illinois

Although plug-compatibility is a useful attribute of an add-on memory, it is not essential; here is a case where the memory of one small computer was doubled in capacity without compatibility, and at low cost as well

Expanding a computer's memory can be highly cost-effective even when memory modules purchased from vendors other than the mainframe manufacturer are not plug-compatible with the mainframe. The lack of compatibility can often require considerable effort to be expended in connecting the new modules to the computer.

Normally, a memory module interfaces to a CPU in a very straightforward manner, necessitating little in the way of complex control circuitry. In a non-compatible expansion built at Argonne National Laboratory, however, some peculiarities of the memory interface made the adaptation more complex than would be likely in other cases. Nevertheless, little difficulty was experienced in making the expansion work.

Add-On Implementation

The computer, a Systems Engineering Laboratories 840MP, has a word length of 24 bits plus a parity bit and a program-protect bit on each word, 26 bits in all. Increasingly sophisticated application for online data collection in a nuclear-reactor physics laboratory[1] necessitated memory expansion from the original 16,384 words to 32,768. GSA-catalog price for this expansion by the mainframe manufacturer is $46,200, plus field-installation charges; even on the used-equipment market, the current price is $16,000.

An additional requirement was to write the program-protect bit separately from data and parity bits in the same word. No compatible memory meeting these requirements was available from any outside vendor.

However, these requirements could be met by a non-plug-compatible memory unit purchased for $6206 from an independent memory manufacturer, who included certain modifications in this price, as described later. This unit was made up of three memory boards each containing a module of 8192 words of 18 bits, a chassis with power supply, a blank board for interface circuitry, and an extender board.

In the expansion modules, each 18-bit word is divided into two bytes which can be read or written separately. Ordinarily, the two bytes are organized as nine bits each, called a 9 + 9 configuration. However, in response to our specifications, the vendor rewired two of the three modules so that in each of them one byte would consist of one bit and the other byte would contain the remaining 17 bits (Fig. 1). The 1-bit "byte" was assigned to the program-protect bit while the remaining byte carried 17 of the data bits for the corresponding word. One module was assigned to the lower 8K of the expansion while the other handled corresponding bits for the upper 8K.

The third module retained the original half-and-half byte division. One byte was assigned to the seven

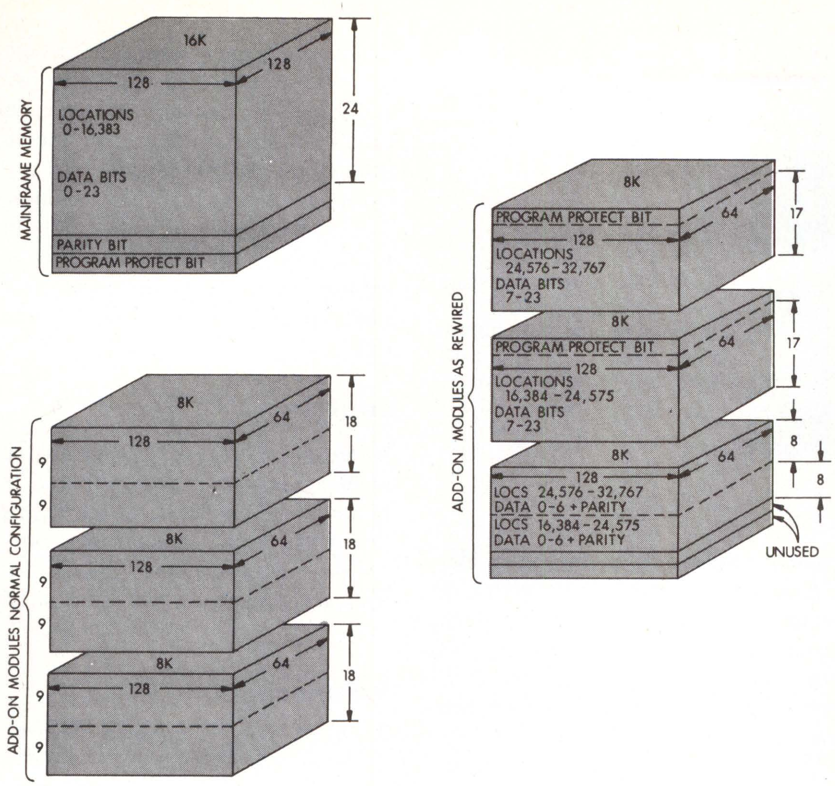

Fig. 1 How modules were rewired. To double the capacity of the main memory, two 8192 x 18 modules were rewired as in this conceptual diagram (bottom right) to hold 17 data bits and the program-protect bit of each word in the expansion. The remaining seven data bits and parity bit of each word were assigned to normal half-and-half configuration of a third module

remaining data bits and the parity bit for a word in the lower 8K expansion, while the other byte of the same word carried the corresponding bits for the word in the upper 8K of the expansion having the same address modulo-8192. Two bits of the third module remained unused.

This new memory has a cycle time of 0.9 μs which is faster than the 1.75-μs cycle time of the CPU and the original memory. Unfortunately, because the CPU is organized completely around the slower cycle, and there is no way to take advantage of that extra speed, the new memory had to be slowed down to keep in step with the rest of the system. A further complication was that the memory input bus, which transmits information from the CPU to the memory, carries both addresses and data at different times in the cycle.

Memory operation for reading is straightforward. When the CPU needs a datum, it gives a read command and places the address on the memory input bus. The memory then performs a read-restore cycle. After the read portion of the cycle is complete, the datum appears on the memory output bus. Although the new memory completes its read operation a little faster than the existing memory, that causes no trouble.

Write operations are a little more complicated. The write command is given at the same point in the CPU cycle as the read command; the memory input bus carries the address as before. The datum to be written does not appear on the memory input bus until one-half cycle later. If the new memory were allowed to perform a clear-write cycle at its own full speed, the datum would not be present when needed for the write portion of the cycle. Therefore, every write operation requires a split cycle; when the write command is given, the memory performs only the clear portion of the cycle (essentially identical to a read cycle except that the CPU accepts no data) and sets a flip-flop. One-half cycle later, when the datum is available, the flip-flop gates the appropriate clock pulse to initiate the write portion of the cycle, after which the flip-flop is reset. Obtaining these cycle-initiating pulses was straightforward from normal control pulses and a few logic blocks.

Because of this CPU's peculiar requirements, it was necessary to actuate the strobe lines for the address and data registers externally, instead of with the module control circuits of the new memory. The address strobe, synchronized with the cycle-initiate pulse, usually gates the 13 low-order address bits into the address registers. However, certain instructions, such as memory increment, execute two successive memory cycles at the same address; since they do not present address information on the memory input bus for the second cycle, the address strobe is inhibited at these times.

The data register strobe occurs at the beginning of the write portion of the write cycle—unless the program-protect bit were found to be on during the clear portion of the cycle and if the CPU indicates that the write operation would constitute a protection violation. Under these conditions the contents of the data register remain unchanged, so that the datum read during the clear cycle is written back during the write cycle.

Byte-select controls of the two modified modules normally select the 17-bit data byte. However, if the program-protect bit is being written, the byte controls are switched accordingly, automatically resetting to the data byte afterward. When writing the program-protect bit, the memory controls inhibit operation of the third module. Byte selection for the third module, which depends on which half of the expansion is being selected, is controlled by the address.

The chassis for the new memory was designed for rack mounting, but was installed facing upward in a vacant space behind a removable blank panel at the right front of the mainframe cabinet (Fig. 2). It was placed in a special holder that allows it to be readily swung forward for maintenance, or removed entirely.

Circuits that transmit data and control signals to and from the new this memory expansion was installed, the system was under a third-party maintenance contract, with a full-time technician employed by the contractor on our premises. With the contractor's assent, this technician was sometimes available for other work, which included installing and debugging the new memory. Today the system is under in-house maintenance.

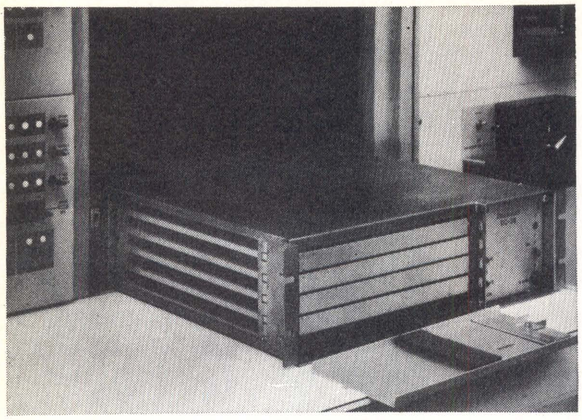

Fig. 2 Expansion chassis. New memory's three modules plus an interface board fit in mainframe cabinet and tilt out for maintenance

memory also transform from the resistor-transistor logic (RTL) of the CPU to the transistor-transistor logic (TTL) of the memory, and vice versa. Signals are transmitted to the memory by discrete transistors driving the line-terminator networks recommended by the memory vendor. Signals are received from the memory through line terminator networks that can directly feed the RTL memory output bus in the CPU. All of these circuits were installed on a special board located in another vacant space in the mainframe and connected to the chassis of the new memory with twisted-pair cables and to the CPU circuits directly.

After the installation was complete, the debugging effort to make the system fully operational required only a few days. At the time this memory expansion was installed, the system was under a third-party maintenance contract, with a full-time technician employed by the contractor on our premises.

Summary

Installing a non-plug-compatible memory is not as forbidding a task as might be expected. In the example described here, the project proved to be successful and, in addition, was accomplished with considerable cost saving.

Reference

1. A. B. Long, "Integrated System for On-Line Computer Acquisition of Data from ZPR-6 and ZPR-9," Argonne National Laboratory, Applied Physics Div, Annual Report, July 1, 1970 to June 30, 1971, ANL-7910, pp 377-381

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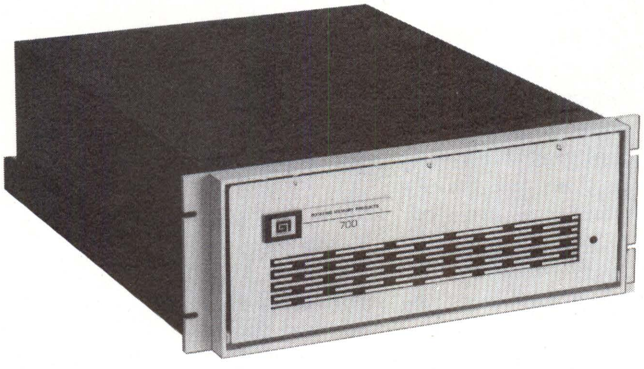

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CIRCLE 48 ON INQUIRY CARD

DESIGN NOTE

POS Cable: A Design Study

Ramesh D. Sheth

Belden Corporation
Richmond, Indiana

Data communication systems of all kinds can benefit from development of low loss, low noise cable designed specifically for the stringent requirements of point-of-sale terminals

A cable design developed for high speed electronic point-of-sale (POS) systems carries signals of up to 10 MHz with less attenuation, less crosstalk, and less noise pickup than the traditional, standard cable designs. The cable is also useful in other data communication systems where long cable runs are necessary, particularly through less than optimum environments, while avoiding at least some of the expense of booster amplifiers. It supercedes older multipair cables—both shielded and unshielded—which served well in lower frequency applications with cable runs of less than 1500 ft, but which exhibited excessive signal losses when used at higher frequencies in lengths of up to 4000 ft. High levels of crosstalk at these frequencies caused excessive error rates even with shielded designs. Similarly, attenuation losses were too high unless costly repeaters were used.

Design Goals

As a result, new cable designs, suitable for operation in the 1- to 10-MHz range over long distances, were required if the new-generation POS systems were to operate efficiently at design capacities. In response to this problem, Belden was requested to provide a low loss, low capacitance, 2-pair POS cable design for such applications. Initial goals were: nominal capacitance between conductors of a pair, 6 to 7 pF/ft; nominal impedance of a pair, 180 Ω; nominal attenuation, 1 dB/100 ft at 10 MHz; crosstalk isolation, 70 dB minimum at 150 kHz; and cable diameter, 0.5 in. maximum.

The cable thus designed is typical of the approach used in designing cable configurations for new or specialized applications. In many instances, previous designs serve as the building blocks for what eventually evolves as the final product. The approach produces several trial designs using existing materials in combinations that have not been used previously, but involves neither basic research nor a technical breakthrough.

The company's 8741 and 9302, both utilizing two pairs of conductors, served as starting points for the POS cable. Physical and electrical characteristics of these standard configurations, along with those of the new cable (150-Ω impedance) that resulted from this design effort, are listed in the Table. Also included for reference are data on a subsequent design (100-Ω impedance).

Both the 8741 and 9302 are miniature configurations utilizing thin-wall (0.015-in.) polyvinyl chloride (PVC) as insulation. The significant difference between the designs is the shield of aluminum-polyester laminate (Beldfoil®) and associated drain wire on the 9302. Shielding minimizes crosstalk in comparison with the 8741, but the higher capacitance of this design results in increased attenuation losses, limiting functional length of the cable.

Attenuation Reduced

To provide reduced attenuation, cellular polypropylene was selected as the dielectric material. With a nominal wall thickness of 0.045 in. and using 22 AWG solid tinned copper conductors, this design yielded a capacitance of 9 pF/ft—sufficiently close to the stated goal. Although cellular polypropylene and cellular

Cable Characteristics

Item	Standard: 8741	Standard: 9302	New: POS 150-Ω Cable	New: (Preliminary) POS 100-Ω Cable
(Physical Design)				
Conductors	22 AWG STC	22 AWG STC	22 AWG STC	22 AWG STC
Dielectric material	PVC	PVC	Cellular polypropylene	Polyethylene
Nominal insulation thickness (in.)	0.015	0.015	0.045	0.019
Number of pairs	Two	Two	Two	Two
Lay of pairs	Same	Same	Each with different lay length	Each with different lay length
Shield	None	Beldfoil[R]	Duofoil[R]	Foil + Braid
Drain wire	None	22 (7 x 30) TC	22 (7 x 30) TC	22 AWG STC
Jacket	PVC	PVC	PVC	PVC
Jacket thickness (in.)	0.028	0.028	0.035	0.033
Cable nominal diameter (in.)	0.201	0.211	0.36	0.3
(Electrical Characteristics)				
Nominal dc resistance of conductors (ohms per 1000 ft at 68°F)	16	16	16	16
Nominal capacitance between conductors of a pair (pF/ft)	22	34	9	15.5
Nominal velocity (V) of propagation (% of velocity of light)	63	60	76	66
Nominal impedance* (Z_0) of a pair (ohms)	73	50	150	100**

*Value of impedance given is calculated using the formula

$$Z_0 = \frac{101600}{V\,(\%) \times C\,(\mathrm{pF/ft})}$$

**Preliminary test data

polyethylene both have favorable electrical characteristics and are frequency-stable over a broad range, the former was selected because of its superior abrasion resistance, durability, and strength.

Decreasing the size of the conductors was considered as an alternative method of achieving reduced capacitance but was rejected because of higher attenuation. A combination of the 9-pF/ft capacitance and a velocity of propagation (76% that of light) for cellular polypropylene yielded an impedance of 150 Ω—an acceptable value. (Designers of high frequency cables often use empirical formulas such as the one for Z_0 [shown in the Table] rather than the familiar expressions based on inductance and capacitance or on open- and short-circuit impedance.)

The reduced attenuation characteristics of the resulting design are compared with the 8741 and 9302 in Figs. 1 and 2 (preliminary test data for the 100-Ω cable are also shown). For example, in a 40-dB system at 10 MHz, the cellular polypropylene-insulated cable will perform effectively at up to 4000 ft; in a 60-dB system at the same frequency, a 6000-ft cable run is feasible. At the 5-MHz frequency, a 40-dB system can be stretched to 5700 ft and a 60-dB system can be extended to more than 8500 ft.

Crosstalk Minimized

To increase crosstalk isolation, a shield was selected consisting of a polyester insulating layer between two sheets of aluminum foil (trademarked Duofoil). This construction provided 100% coverage, and superior shielding effectiveness compared with designs that utilized a single layer of aluminum. Varying the lay length of each conductor

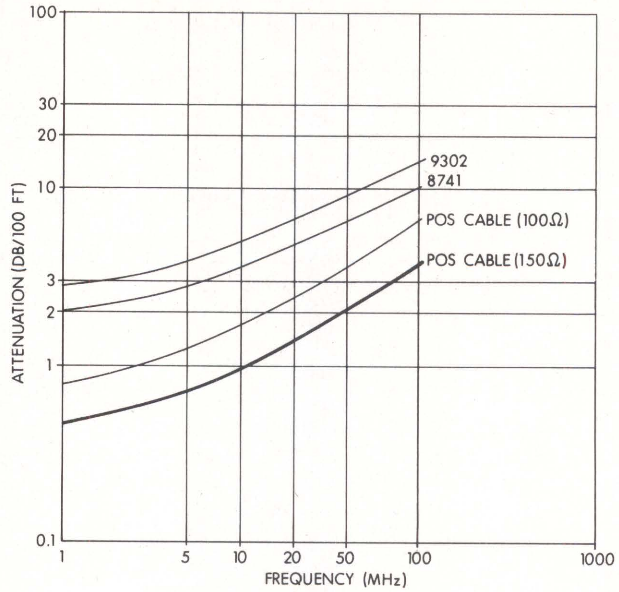


FIG. 1

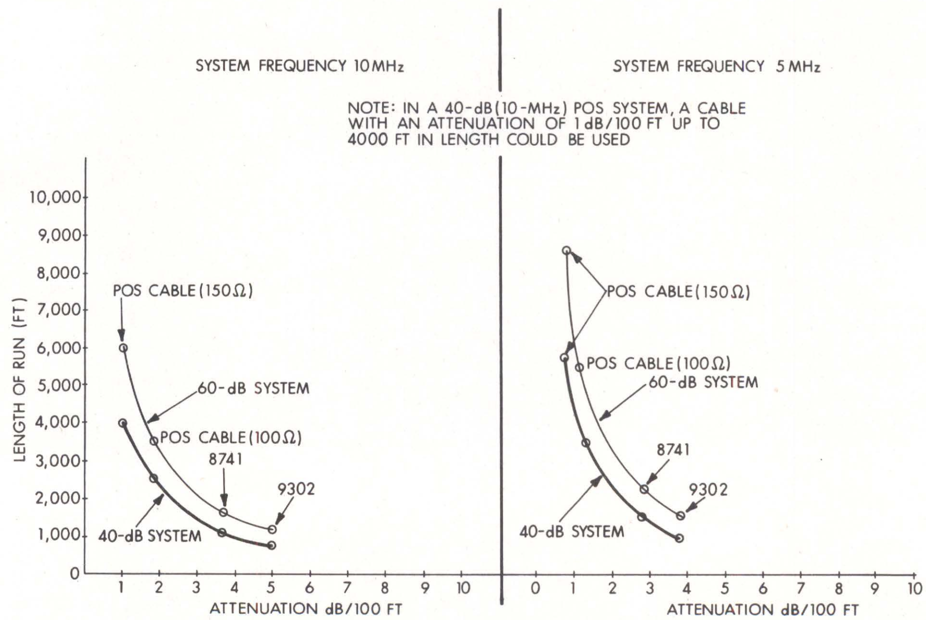
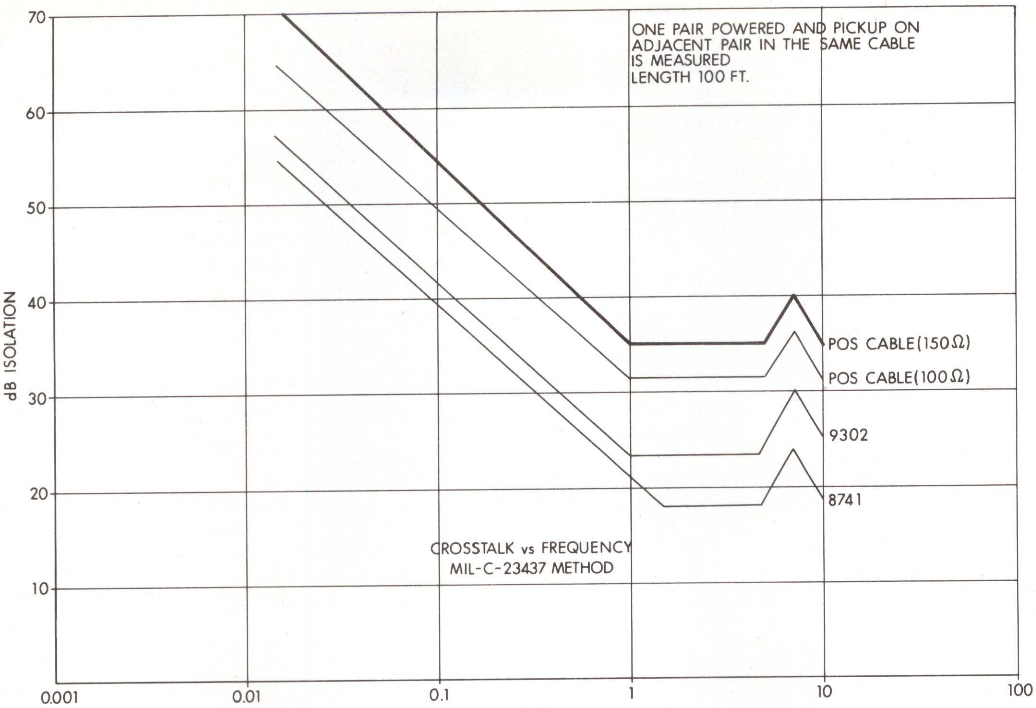


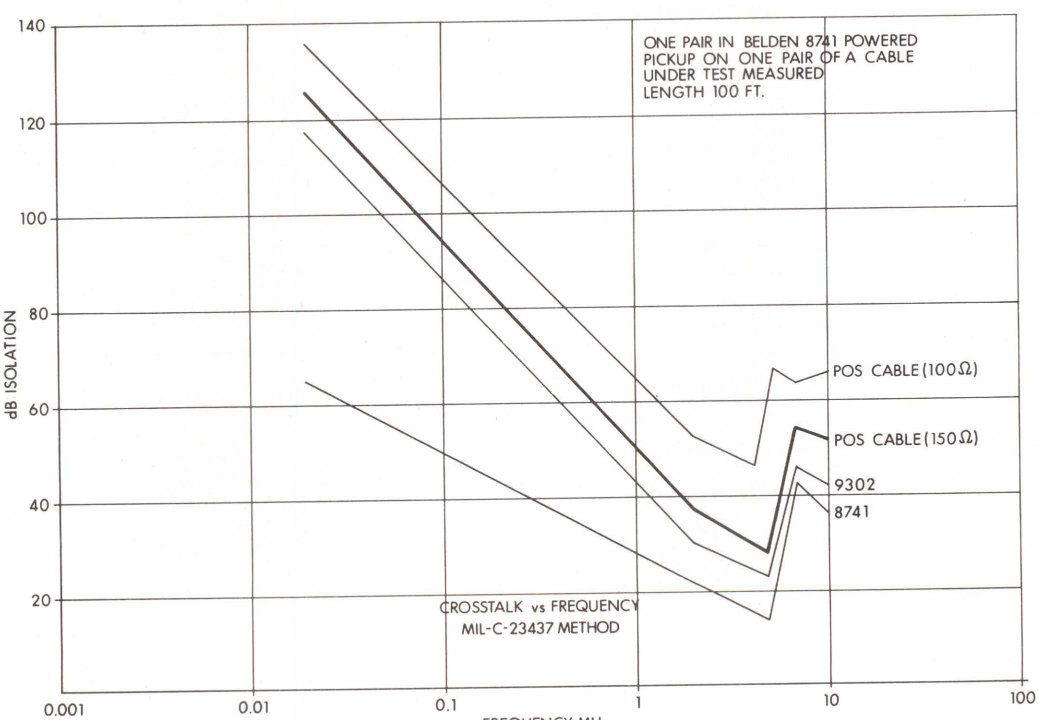
FIG. 2

Figs. 1-4 Old and new cable characteristics. Graphs show, in order, attenuation as a function of frequency (Fig. 1), cable length as a function of attenuation (Fig. 2), and crosstalk isolation vs frequency (Figs. 3 and 4). Clearly, the Duofoil[R] shield is less subject to crosstalk



ONE PAIR POWERED AND PICKUP ON ADJACENT PAIR IN THE SAME CABLE IS MEASURED LENGTH 100 FT.
dB ISOLATION
70
60
50
40
30
20
10
POS CABLE(150Ω)
POS CABLE(100Ω)
9302
8741
CROSSTALK vs FREQUENCY
MIL-C-23437 METHOD
0.001
0.01
0.1
1
10
100
FREQUENCY MHz

FIG. 3



ONE PAIR IN BELDEN 8741 POWERED PICKUP ON ONE PAIR OF A CABLE UNDER TEST MEASURED LENGTH 100 FT.
dB ISOLATION
140
120
100
80
60
40
20
POS CABLE(100Ω)
POS CABLE(150Ω)
9302
8741
CROSSTALK vs FREQUENCY
MIL-C-23437 METHOD
0.001
0.01
0.1
1
10
100
FREQUENCY MHz

FIG. 4

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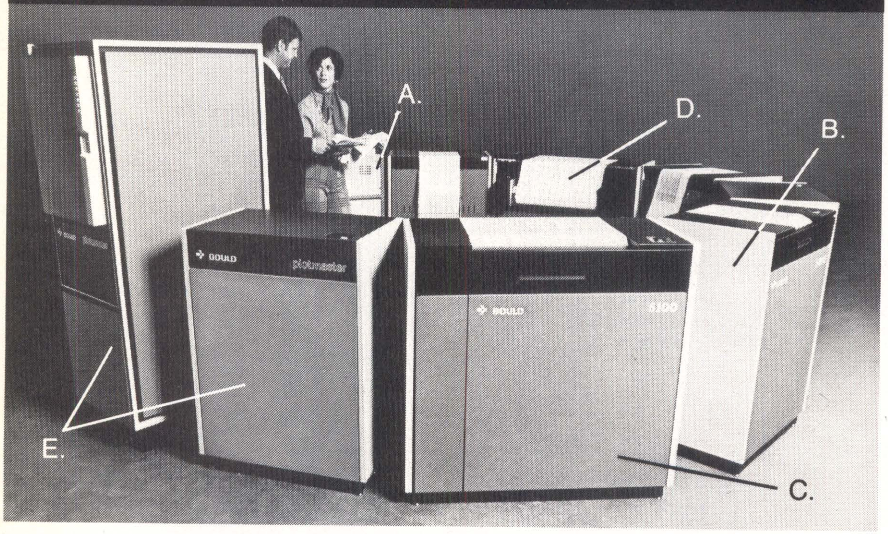

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pair also contributed to increased isolation between pairs of the same cable. As with the 9302, a drain wire was applied over the shield to facilitate termination.

Using the MIL-C-23437 test method, Figs. 3 and 4 compare crosstalk isolation characteristics of the 8741, 9302, and new POS cable design (also included are preliminary test data for the 100-Ω cable). In Fig. 3, one pair of each of the three cable samples is powered, and crosstalk is measured in the adjacent unpowered pair. The chart indicates a minimum isolation value of 35 dB in the 1- to 10-MHz range, compared with the minimum of 23 dB achieved by the standard shielded design of the 9302. Fig. 4 utilizes one powered pair in the 8741 as the frequency source for measurement of crosstalk in one pair of the other cable samples. As in the previous test, the degree of isolation provided by the Duofoil shield indicates clearly the superior resistance of the resulting design to crosstalk. (Note: Crosstalk values may vary, depending upon the method used for measurement. Values presented here were obtained using the MIL-C-23437 test method.)

Summary

Availability of the new cable enables users to take better advantage of the greater speeds and capacities of many POS systems in use or planned by leading retailers. Experience gained in this design program can also serve as the basis for creating new cable designs. For example, hardware manufacturers are presently investigating equipment that will require cables to comply with a nominal impedance requirement of approximately 100 Ω. Designs utilizing solid polyethylene (see Table and Figs. 2 through 4) as the insulation material already have been developed to meet this requirement.

Because of the rapidly changing nature of the electronics industry in general, and POS systems and other data transmission applications in particular—for example, electronic fund transfer systems and customer-bank computer terminals, it is vital that system manufacturers consider interconnecting cable requirements at the beginning of the system design sequence. □

CIRCLE 49 ON INQUIRY CARD

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DESIGN NOTE

Solid-State Analog Switch Matrix Replaces Relay and Crossbar Selectors

Ronald W. Embley

Electronic Associates, Incorporated
West Long Branch, New Jersey

Eight individual analog voltage inputs can be connected separately to eight outputs with a switch matrix to permit fully automatic patching in a hybrid computer

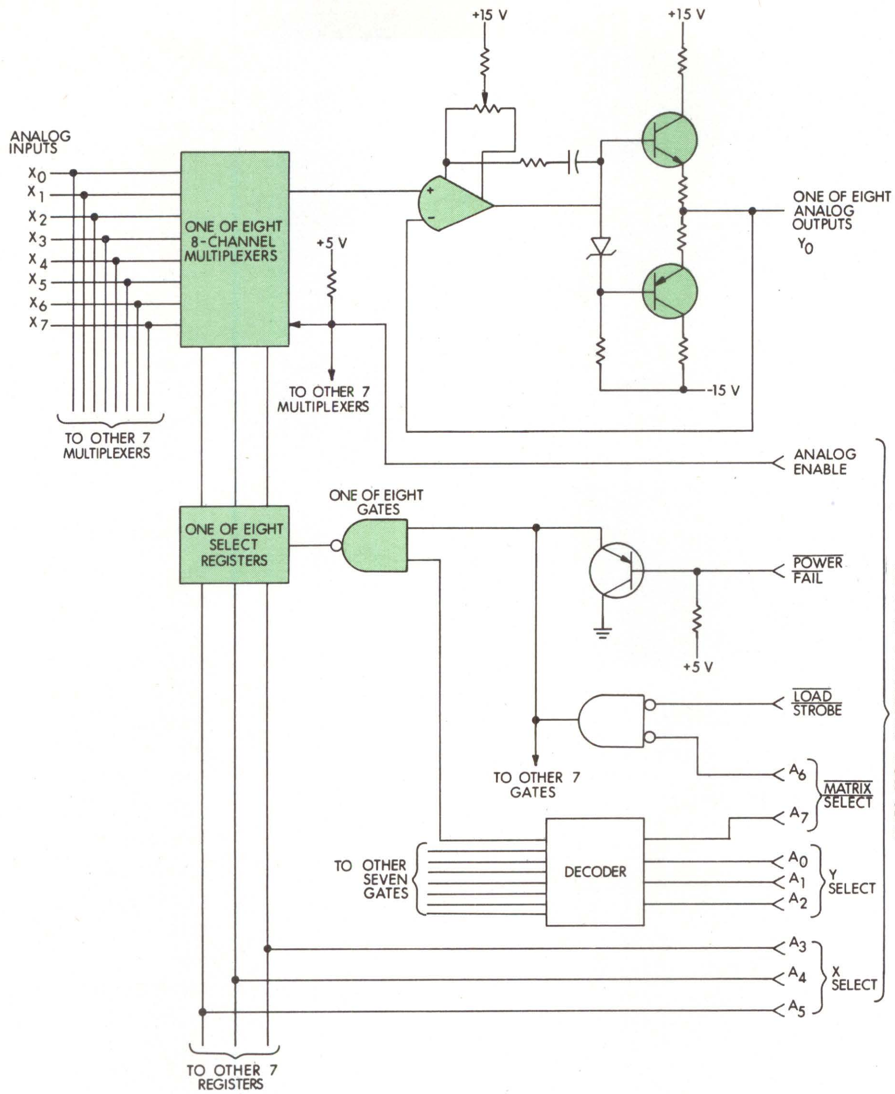
An 8-by-8 solid-state matrix for switching analog voltages has been designed with complementary metal-oxide semiconductor (CMOS) multiplexers and CMOS logic to replace relay designs and crossbar switches. When power is supplied in part by a 5-V battery, the circuit is nonvolatile, maintaining any desired switch selection in the event of a power failure. Such nonvolatile operation is not feasible when other types of integrated circuits are used, because they draw more current than can conveniently be supplied by a small battery; meanwhile, the switching functions are much faster than with traditional electromechanical devices.

In the matrix (see Figure), any analog output, Y_n, can be connected to any analog input, X_n. Only one input can be selected for a given output, but any one input can be connected to one or more outputs, if desired. Each 8-channel multiplexer drives a noninverting buffer amplifier with a high input impedance and low output impedance. Each multiplexer's input channel is selected by a register of three latches (in a quad package), the states of which are decoded internally in the multiplexer.

Making a Connection

An 8-bit word from a computer or other digital controller establishes a single X-to-Y connection. In this word, bits A_0, A_1, and A_2 are decoded to select a single Y output, while bits A_3, A_4, and A_5 identify the particular X input to be connected to that output. Bits A_6 and A_7 permit up to four independent switch matrices to be used together in four separate 8-by-8 arrays or, with common inputs, in one 8-by-32 array.

The three bits that identify one of the eight X inputs are routed to all eight 3-latch registers serving the eight multiplexers. These latches are set by a strobe pulse from the computer that is gated to only one of the eight latch groups by the output of the Y-decoder; the latches in that group change state as required to agree with the state of the three X-input lines. They do so because they are D-type flip-flops, which acquire the binary state of their input lines with each clock pulse (strobe pulse) and retain that state, regardless of changes in the input lines, between clock pulses. One 8-bit con-



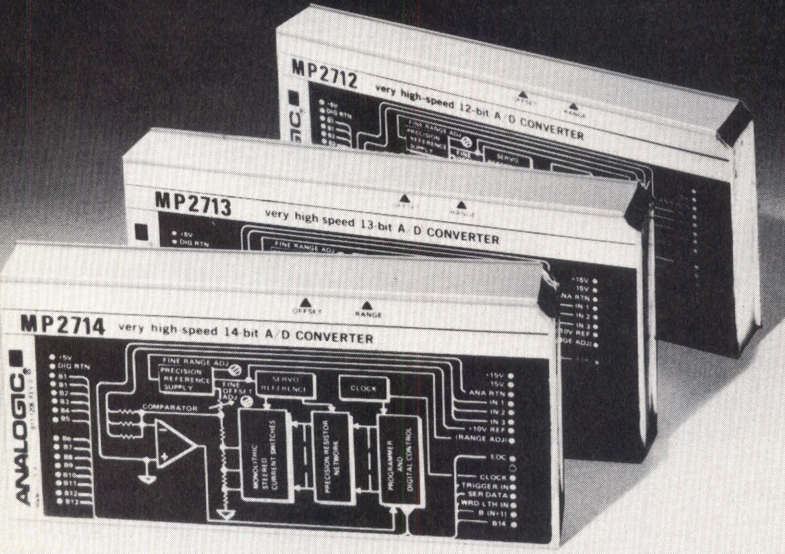
Matrix replaces crossbar switch. Any of eight X inputs can be connected to any of eight Y outputs, including one X to two or more Y's (but not two X's to one Y). The connection is nonvolatile if critical circuits are battery powered; CMOS logic permits a small battery to do the job. Connection data arrive on lines A_0 through A_7 from a digital computer or controller; reconfiguration is fast enough to allow a time-shared hybrid system

trol word followed by one strobe pulse establishes one input-to-output connection; the cycle is repeated seven more times to connect each of the outputs to the desired inputs.

If the controlling computer detects an incipient total power failure, the Power Fail line goes low, blocking the strobe pulse and thus inhibiting any erroneous data loading. Meanwhile, the CMOS latches, supplied with battery power, retain their previous state during power failure. If not required, this feature may be bypassed by connecting the $+5\text{-}V_a$ power bus serving the latches to the $+5\text{-}V_b$ power lines serving the other circuits.

All eight multiplexers can be disabled by a signal on a line called Analog Enable. This line is at a logic high during normal operation; if it is brought low, the outputs all saturate at approximately -13 V.

Analogic A/D Converters give you a bit more for less



If you're counting on every bit that you've specified . . . specify the new 2700 Series 12, 13 and 14-bit A/D converters.

Relative accuracies range from 0.004% for 14-bits to 0.012% for 12-bits, conversion times from less than 4μsec to 10μsec and differential linearity tempco of all three models is less than 3ppm/°C. In other words, you can get *true* 12, 13 and 14-bit performance even under worst-case conditions! The price for this outstanding performance? About half what you would expect to pay ($204 for the MP2712, $272 for the MP2713 and $368 for the MP2714, in 100s).

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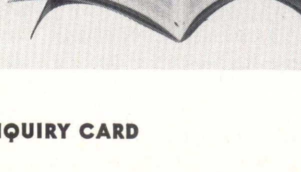

ANALOGIC®
. . . The Digitizers

Parts and Performance

The eight multiplexers are Siliconix type DG508C or equivalent. Resistors and diodes in series with their power leads protect them from catastrophic failure caused by voltage spikes during power sequencing. All logic functions are performed using RCA's 4000 series CMOS circuits or equivalent, while the operational amplifiers are Analog Devices AD518K. They have a guaranteed common-mode rejection ratio of 90 dB and an output offset voltage that, with temperature, changes less than 15 μV/°C. An output stage with each amplifier, made with discrete components, increases the capacitive load-driving capability from 100 to over 1000 pF. The output stage shows no distortion at frequencies as high as 100 kHz and is immune to momentary short circuits. The circuitry fits on a 4.3-by-10.-in. printed-circuit board with edge-connector mating fingers.

Circuit performance of a simulated 3-level matrix was measured on three matrix cards connected in cascade with the buffer amplifiers present on only the third level or output card. The measurements, with an input of 20 V pk-pk at 1 kHz, showed a phase shift of 0.03 to 0.05 deg, crosstalk of 94 dB down when all but one input are grounded and the measurement made on outputs not connected to that input, a dc offset adjustable to 0 ±20 μV, and a gain of 1 ±0.003%.

One major application for the 8-by-8 analog switch matrix is to replace the manual patch panel on an analog computer, so that patching becomes completely automatic.* The resulting "auto-patched" analog/hybrid computer not only relieves the programmer of the burden of manual patching, but provides fast problem-turnaround times (on the order of several milliseconds), which enables analog/hybrid simulations to be time-shared.

A prototype system employing these 8-by-8 switches is in use on an EAI 681 analog/hybrid computer and is presently being evaluated in the EAI computer laboratory. □

* G. Hannauer, "Automatic Patching for Analog and Hybrid Computers," *Simulation*, May 1969, pp 219-232

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KIT	ASM	
$350	$520	**ONE-CARD COMPUTER:** Motorola 6800 microprocessor, 4K RAM, 512 bytes EPROM (containing a Program Development System), a REAL-TIME CLOCK, 16 LINES OF DIGITAL I/O, hard wired ROM Monitor, and a serial type interface. This is the 100-quantity price, available in quantaties of one, or an evaluation basis.
522	622	**CPU BOARD:** Motorola 6800 microprocessor, 4K RAM, 1K EPROM (containing an EDITOR, ASSEMBLER, DEBUGGER, COMMAND LANGUAGE, CASSETTE LOADER, DUMPER, UTILITIES), and a REAL-TIME CLOCK.
860	1400*	**SPHERE 1:** Includes the CPU BOARD described above, plus 512 character video with full ASCII keyboard and numeric/cursor keypad, power supply, chassis, manuals and associated parts.
$999	$1499*	**SPHERE 2:** Includes all features of SPHERE 1, plus serial communications and audio cassette or MODEM interface.
1765	2250*	**SPHERE 3:** Includes all the features of SPHERE 2, plus memory totaling 20K which is sufficient to run full extended BASIC Language.
6100	7995*	**SPHERE 4:** Includes all of the features of SPHERE 3, except the cassette has been replaced by an IBM-compatable Dual Floppy Disk System. This system includes a Disk-operating System and BASIC Language and a 65 LPM line printer.
(various)		**OTHER SPHERE PRODUCTS:** Light pen option; full color and B/W video graphics system; low cost Dual Floppy Disk System; and full line of low cost peripherals.

*This ASSEMBLED SPHERE System includes the complete chassis, and video monitor as pictured below.

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CIRCLE 52 ON INQUIRY CARD

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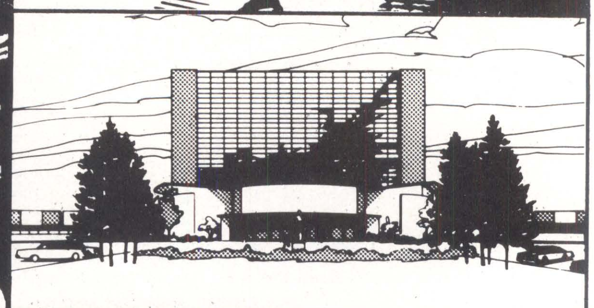
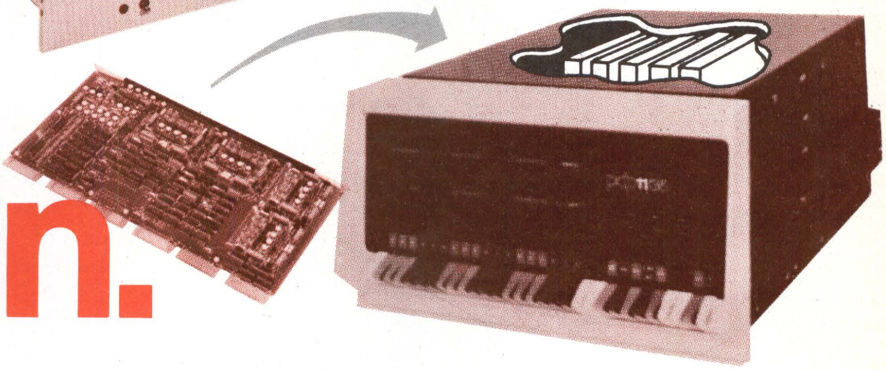
Danny Thomas, Founder



Add-on.

Add-in.



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- PDP-8/F
- PDP-8/M
- PDP-11/05
- PDP-11/10
- PDP-11/35
- PDP-11/40

DCC
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TECH BRIEF

Digital Second-Order Phase-Locked Loop

The Problem

The relative Doppler shift of a telemetry subcarrier, previously thought to be 1 x 10^{-5}, has been found to be 1 x 10^{-4} in some instances. The Doppler shift of the subcarrier induces a phase error bias in the receiver subcarrier timing that increases with increasing Doppler shift. Because of these facts, a first-order digital phase-locked loop (DPLL) is not adequate for tracking the signal without an appreciable timing error and, in fact, will not lock at a relative frequency offset of 2 x 10^{-4}.

The Solution

Actual tests with a second-order DPLL at a simulated relative Doppler shift of 1 x 10^{-4} produced phase lock with a timing error of 6.5 deg and no appreciable Doppler bias. Thus the loop appears to achieve subcarrier synchronization and to remove the bias due to Doppler shift in the range of interest.

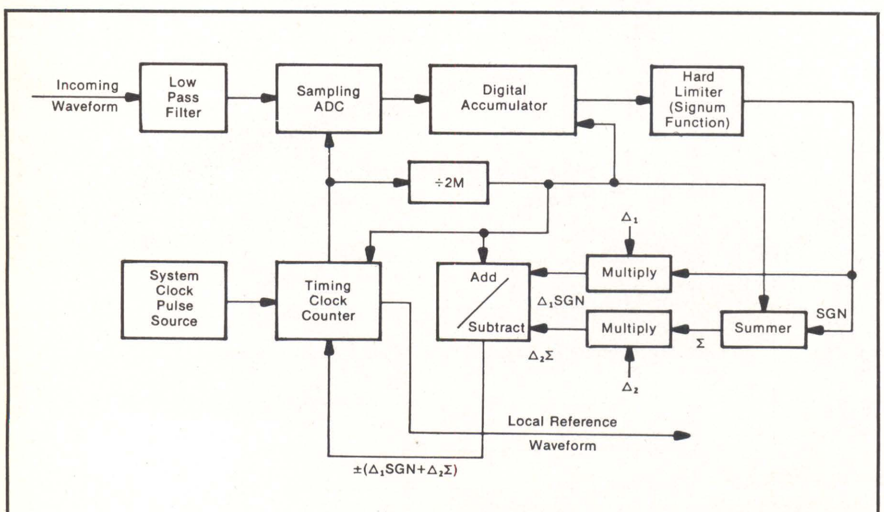
How It's Done

Based on the fact that an analog second-order PLL has no static phase error in the presence of Doppler shift, a linear, analog PLL model, equivalent to a second-order digital PLL was analyzed and constructed, as shown in the diagram. The loop operates in the same manner as a first-order DPLL, except for the addition of the summer branch of the loop filter. The incoming waveform is assumed to be composed of a squarewave subcarrier of amplitude A, with period T_{SC}, and white Gaussian noise of 2-sided spectral density $N_o/2$. The low-pass filter cuts off at a frequency of W Hz. The sampler obtains a sufficient number (16) of equally spaced samples per subcarrier cycle to represent the signal adequately.

These samples are then converted to digital format (a 4-bit word in this case) by the analog-to-digital converter (ADC). The ADC (which can be thought of as a phase detector) also selects a sample corresponding to the nominal center of the subcarrier transition (zero crossing) every subcarrier period. After accumulating M of these transition samples in the digital accumulator, the accumulation is passed to the hard limiter, which implements the signum (SGN) function. The output of the hard limiter, SGN, which is either +1 or −1, is multiplied by Δ_1 fractions of a subcarrier cycle (FSCC) and then increments the clock timing by $2\pi\Delta_1$ radians. Simultaneously, the sign of the accumulation is added to the summer of the loop filter, and an output equal to Δ_2FSCC, times the value of the summer, increments the clock or transition sampler timing by $2\pi\Delta_2$ radians.

The number M largely determines the bandwidth of the loop and is here chosen for convenience to be equal to the number of subcarrier waveform cycles per data bit period. The values of Δ_1 and Δ_2 are each equal to some number of fractions of a subcarrier cycle and may each be selected as required, the only constraint being that $\Delta_1 > \Delta_2$.

In summary, then, the loop operates as follows: The phase detector ADC/accumulator produces an output every M subcarrier cycles, which is then fed to the filter. The filter, in turn, controls the time phase of the sampler via the clock so that the timing is updated by (Δ_1SGN + $\Delta_2\Sigma$) times 2π radians every M subcarrier cycles.



Note

Requests for further information may be directed to Technology Utilization Officer, NASA Pasadena Office, 4800 Oak Grove Dr, Pasadena, CA 91103. Reference: TSP74-10274.

Patent Status

This invention has been patented by NASA (U.S. Patent No. 3,777,272). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to Patent Counsel, NASA Pasadena Office, 4800 Oak Grove Dr, Pasadena, CA 91103. Source: Jack K. Holmes, Christopher Carl, and Carl R. Tagnelia of Caltech/JPL, under contract to NASA Pasadena Office (NPO-11905).

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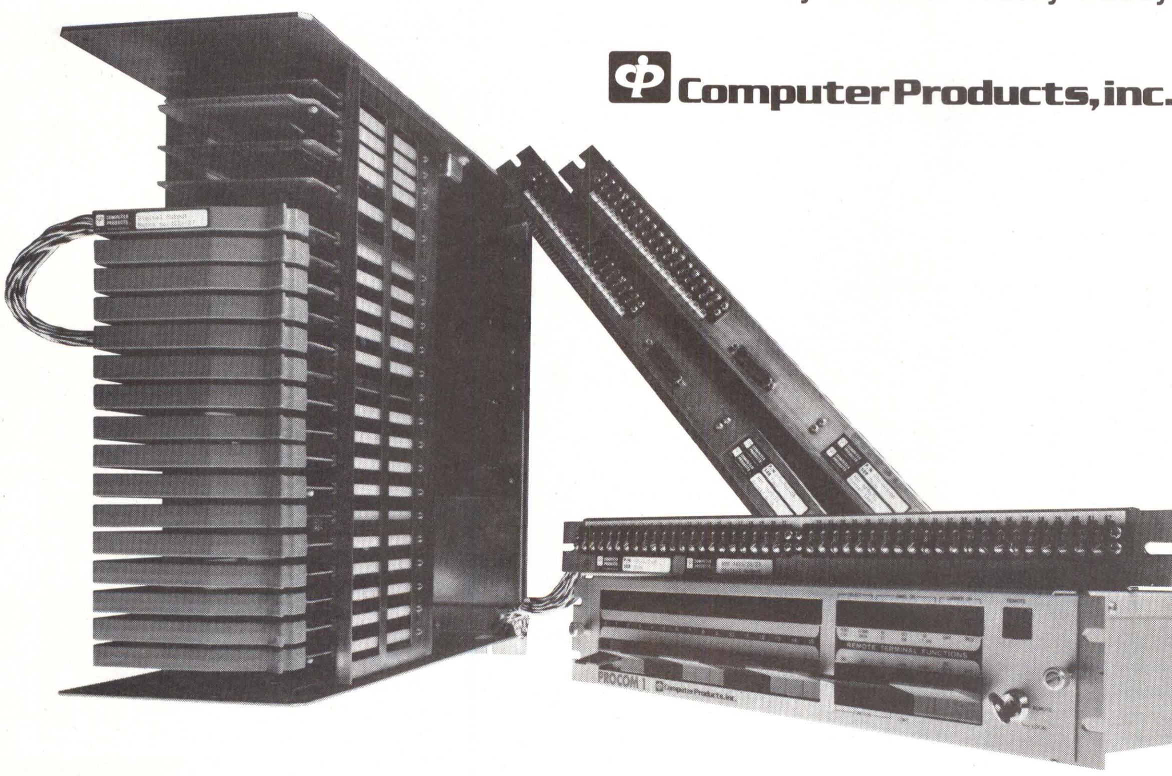

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CIRCLE 50 ON INQUIRY CARD

One-Card µComputer Expands to Four Higher Levels

Through reduction in system circuitry, the Sphere 1 computer system series, introduced by Sphere Corp, 791 S 500 West, Bountiful, UT 84010, features what is claimed to be exceptional cost-effectiveness—achieved, for example, with the use of one add-on memory board which supports 4, 8, 12, or 16 kilobytes of dynamic random-access memory (RAM) rather than use of four 4-kilobyte memory boards and a motherboard; power supply contained in a separate chassis to eliminate a common source of heat; use of a standard TV for display; replacement of the front console with a TV terminal; improved read-only memory (ROM) program; and central processing unit (CPU) card packaged to provide all the basic functions required by a useful system, thereby eliminating extra printed circuit (PC) boards. Also, seven additional parallel terminals plus eight serial terminals can be supported.

The One-Card Computer—the basic OEM version—uses a Motorola 6800 microprocessor as its CPU. Memory is 2107A-type 4-kilobyte dynamic RAM; all refresh circuitry is included on the CPU board. For use in a standalone situation, the system can include 16 programmable input/output (I/O) lines; four additional control lines which may by used as interrupt detection are also contained on the board. Erasable programmable ROM (p/ROM) contains a program development system consisting of a debugger, assembler, editor, 16-bit arithmetic, and ASCII conversion routines. Also featured are a real-time clock and power-on reset. Price of the One-Card Computer in kit form is $350; assembled $520.

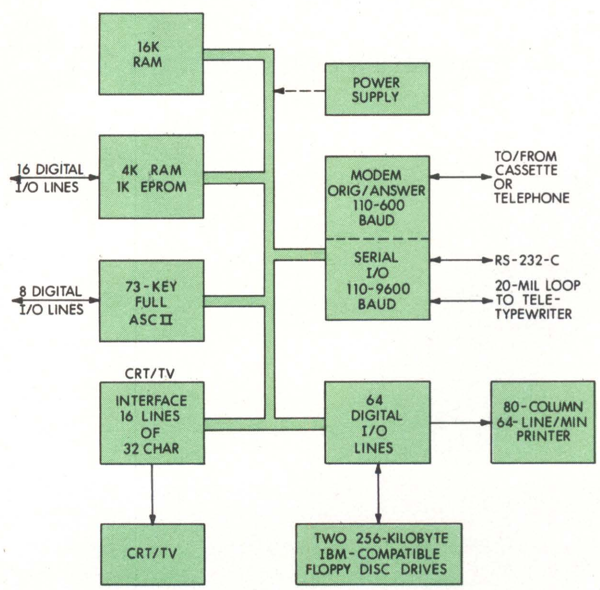
For the user involved in light process control, experimentation, and some educational applications, SYS1 contains all One-Card Computer features plus a CRT terminal which incorporates a standard alphanumeric keyboard with numeric keypad. Its 512-char display is arranged as 32 char/16 lines. The system is equipped with a power supply and operator/reference manual. In kit form, SYS1 is available for $860; assembled, for $1400.

In addition to all features mentioned thus far, SYS2 includes a module equipped for communications to other devices over serial lines, such as a telephone. It accepts data in 8-bit parallel format from the CPU and transmits them serially with one or two start bits and a stop bit. The system also features a module containing a complete originate/answer modem; the device has additionally been adapted to operate with an audio cassette interface. SYS2 kit is $999; assembled, $1499.

The next-advanced version—SYS3—adds a 16K memory board plus full-extended BASIC language programming. Kit price is $1765; assembled, $2250.

Finally, the high-end version—SYS4—incorporates an IBM-compatible dual floppy disc unit plus disc operating system; an 80-col, 65-line/min. dot matrix printer; plus necessary interfaces. Prices are $6100 (kit) and $7995 (assembled).

Circle 170 on Inquiry Card



Sphere SYS4 high-end microcomputer system, incorporating features of basic One-Card Computer plus those of SYS1, -2, and -3, as well as a dual floppy disc unit with disc operating system; line printer; and interfaces

Real-Time µComputer System Features Low Cost Dual-Disc Mass Storage

PDP-11V03 is a microcomputer system with operating system and high level languages, mass storage, and terminal. The low-end, real-time system features large scale integration (LSI) technology and uses the 400+ instruction set of the PDP-11/40. Introduced by Digital Equipment Corp, Maynard, MA 01754, the standard system utilizes RXV11 dual floppy disc drives for online mass storage (512 kilobytes). Average access time is 483 ms. Data are transferred between disc and microcomputer over bidirectional lines at 10 kilobits/s.

Operating software is provided through the disc-based RT-11 system, which can be used to develop and

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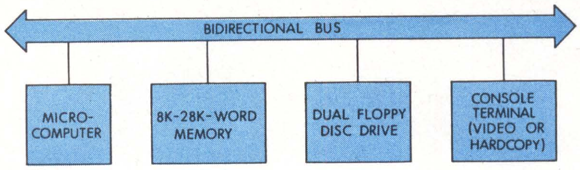


PDP-11V03 microcomputer system, which utilizes dual floppy disc drives for online mass storage of 512 kilobytes of data, and includes real-time operating system

operate user programs written in FORTRAN IV, BASIC, or machine language. It also includes program modules for software debugging, editing, file maintenance, library access, and utility program operations.

Track-to-track move time for each drive is 10 ms, plus 20 ms settling if the system is to perform either a read or write operation. Rotational speed of the diskette is 360 rpm, which results in an average latency time of 83 ms. During a sequential access, the entire diskette can be read in approximately 30 s.

Each disc contains 77 26-sector tracks; each sector stores 128 bytes, for a total formatted capacity of 256 kilobytes/diskette. Given the absolute sector address, the RXV11 locates the desired sector and performs the indicated function. The system automatically verifies head position and generates and verifies the cyclic redundancy check character. In addition, it reads diskettes written on other standard floppy disc equipment, and vice versa.

For input/output communication, users are offered a choice of either the DECwriter II LA36 30-char/s hardcopy terminal or the VT52 DECscope video terminal which displays 24 lines of upper/lower case text at user-selectable speeds of up to 960 char/s.

Circle 171 on Inquiry Card

μComputer Packages Ease Conversion to Process Control

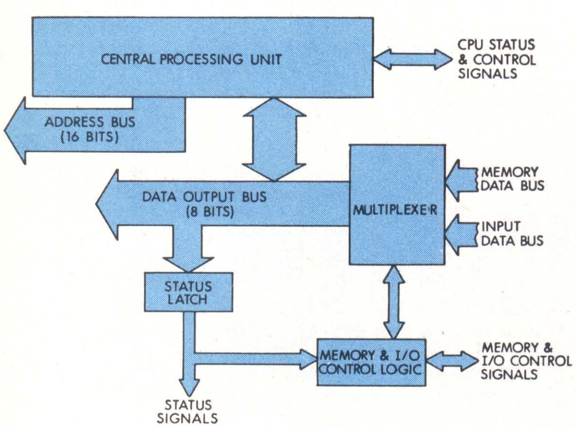
Easy to build into new plant operations or add to existing facilities, for process or numerical control, quality control, materials handling, switching, data collection/logging, and the like, the M-800 series of general-purpose desktop, rack-mounted, and NEMA-enclosed programmable microcomputers from Control Logic Inc, 9 Tech Circle, Natick, MA 01760 can handle 256 inputs and 256 outputs, with a control cycle time of less than 10 μs. Of modular construction, which enables simple card replacement, each unit is organized around an 8-bit central processing unit (CPU) with supporting control logic. The basic processor consists of a CPU, memory and input/output (I/O) control, and a data bus/multiplexer; four system buses for control and communication—input data, memory data, data output, and address—originate and terminate in the processor.

Maximum memory capacity is 64 kilobytes; instruction execution cycle times are 5.5 to 7 μs. Inputs and outputs can be both digital and analog; they handle 24-, 120-, and 220-V relay voltages, 5 Vdc for instrumentation, serial parallel, and decimal data, binary or binary-coded decimal, as well as analog input directly. Virtually any peripheral interface can be accommodated.

For noisy environments, signal conditioning is available through opto-isolation. Brownout protection and power line filtering are optional.

A utility software library includes a loading/debugging program, text editor, resident assembler, cross assembler, and programmable read-only memory programming software. Special software is available for test and diagnostic programs, tape conversion programs, multiply/divide packages, and floating-point packages.

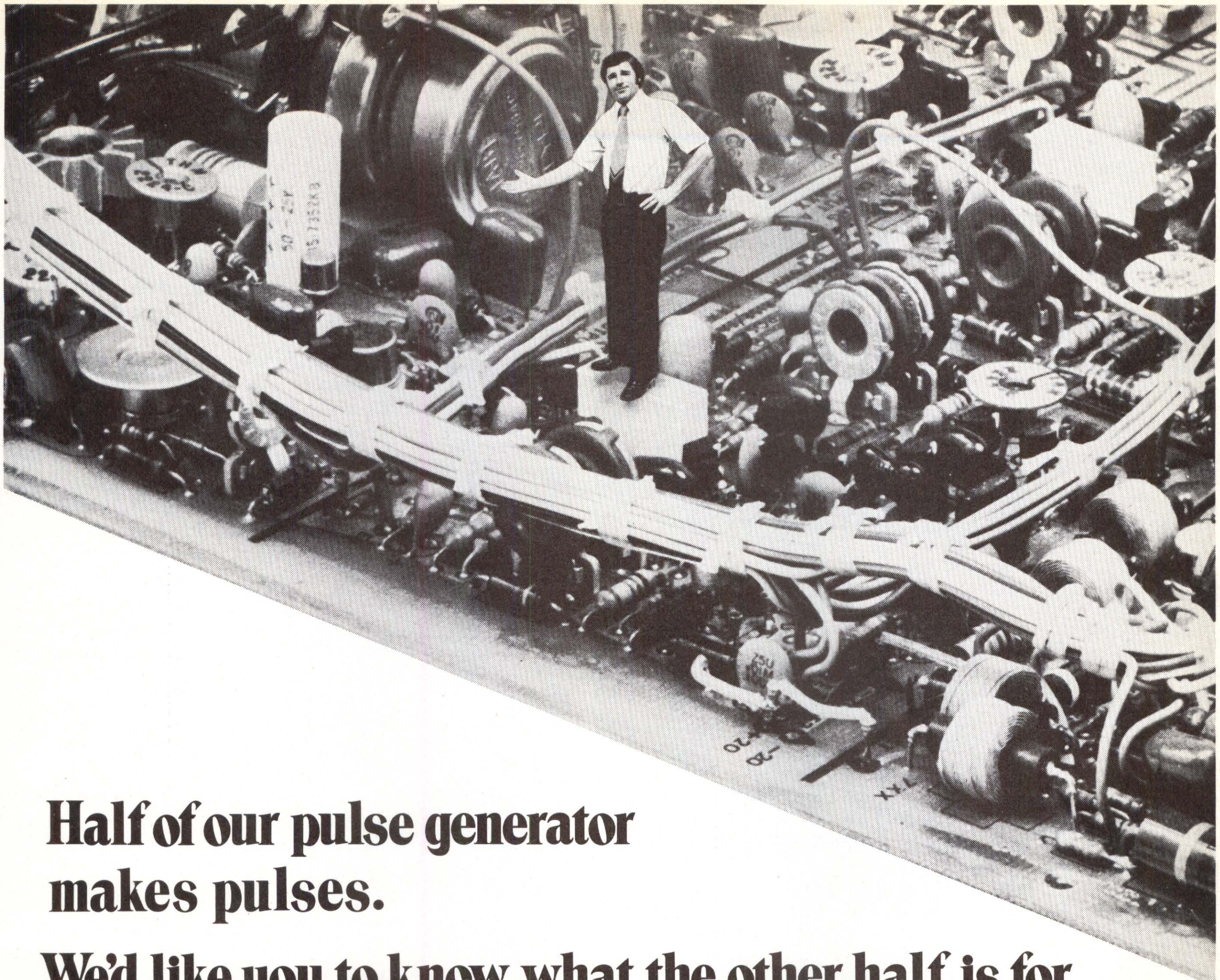
Circle 172 on Inquiry Card



M-800 basic processor, which comprises CPU, memory and I/O control, and a data bus/multiplexer. System buses for control and communication originate and terminate here

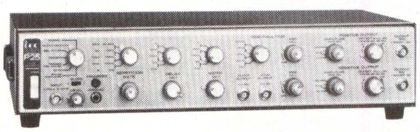
2-Chip μComputer Can Outperform 8-Chip Units

A 2-chip microprocessor system has been designed for OEMs requiring complete microcomputer capability—for a total component cost of less than $35. The high speed PPS-4/2 from Rockwell International Corp, Microelectronic Device Div, 3310



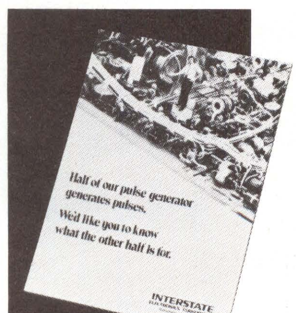
Half of our pulse generator makes pulses.

We'd like you to know what the other half is for.



Pulse generators make pulses — everybody knows that. The half everybody **doesn't** know about is that today's general-purpose pulse generators (like Interstate's SERIES 20) can:

1) **Make your life easier.** With Interstate's constant duty cycle mode, for example, you don't have to reset width and pulse period every time you change the frequency when testing a differential amplifier or an analog computing circuit over a wide range of frequencies. The width-to-period ratio remains constant as you change the frequency. Much easier.
2) **Give you an infinitely more versatile pulse.** Clock and sync outputs on Interstate's SERIES 20 Pulse Generators are squarewaves, instead of those other skinny, 10-nanosecond trigger pulses. So when you're testing low-speed stuff, like electromechanical machines or reed relays, or even some of the new microprocessors, you won't have to keep switching the scope over to high speed to make sure the trigger is there. Interstate's sync pulse is readily visible — and immediately usable.
3) **Allow you to use the pulse generator for other jobs.** SERIES 20's pulse amplifier mode can restore levels and transition times in MECL testing, for instance, so you can avoid having to jerry-rig some complex kluge of equipment.



Put the other half of your pulse generator to work. Interstate has just produced "Today's General-Purpose Pulse Generator Report" in which our SERIES 20 Pulse Generators, together with the major pulse generator models in the 50 MHz, 3.5 ns rise/fall time, 10 V output (into 50 ohms) category, are detailed and cross-compared, and application notes reveal methods and techniques for practical pulse problem-solving.
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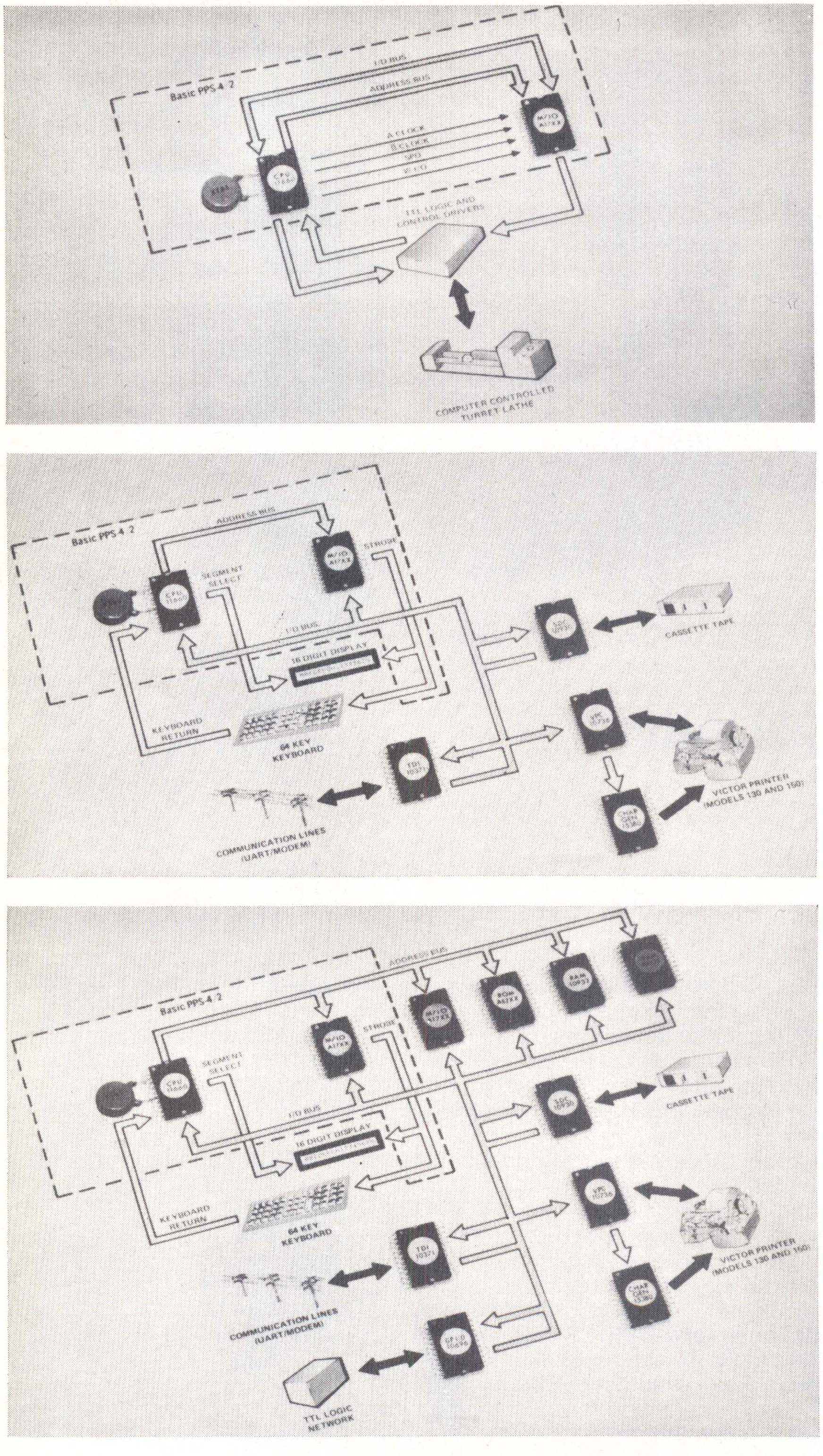


Minimum: complete LSI microcomputer (top), medium: PPS-4/2 6-circuit unit (center), and maximum: 11-circuit -4/2 (bottom)

Miraloma Ave, PO Box 3669, Anaheim, CA 92803 consists of one chip with clock, central processing unit, and 12 input/output (I/O) lines, and a second chip with 2K x 8 read-only memory, 128 x 4 random-access memory, and 16 bidirectional I/O lines. Operating at a 5-μs cycle time, the system is claimed to outperform many 8-bit microcomputers; addition of two 8-digit numbers requires only 240 μs, for example. It is instruction and bus compatible with the PPS-4 microprocessor, so that all 17 I/O, memory, and peripheral controller chips now provided can be used with the -4/2.

Through use of the 28 I/O lines available, a complete system, such as a credit verification terminal with keyboard and display functions, can now be implemented with the two chips; or, a complete electronic cash register implementation requires only three metal-oxide semiconductor chips, the -4/2, and a printer controller chip.

"Use of the -4/2 in industrial control applications is virtually unlimited," states J. E. Bass, director-microprocessor/OEM marketing. "With 28 independent, TTL-compatible I/O lines and 2K x 8 ROM capability, many applications now become 2-chip solutions."

Evaluation boards are being made available this month, and full production quantities will be ready in January.

Circle 173 on Inquiry Card

Kit Evaluates Microprocessors

Evaluation of its 2-chip F-8 microprocessor can now be performed with the F-8 microcomputer kit, according to Mostek Corp, 13300 Branch View Lane, Dallas, TX 75234. A finished printed circuit (PC) board allows component assembly to take no longer than 30 min. Then, with user-supplied teletypewriter or CRT terminal, the designer can write, execute, and debug F-8 programs.

The kit also comprises the microprocessor circuits: a central processing unit, program storage unit in which resides a firmware program that provides immediate system intelligence, memory interface, plus 1K x 8 of static random-access memory. In addition, two CMOS buffers and a 2-MHz crystal are included. Documentation support includes assembly instructions and sample programs, programmer's guide, and a data sheet manual.

Kit applications can be further user-defined with the 24 lines of input/output available from the PC board.

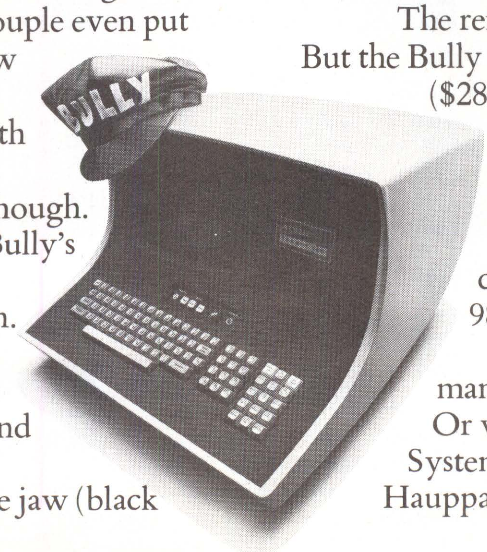
Circle 174 on Inquiry Card

"Sure, my Bully's a competitive terminal. But where's the competition?"

Being the Bully's manager is no picnic, lemme tell ya.

Look. I got a terrific TTY terminal here, ready to take on everybody and his brother and all of a sudden, it's Philly-on-Saturday-night.

Sure, I've seen a lot of tough-talking terminal ads. A couple even put up a good front. But show me one terminal that'll even climb in the ring with my boy these days.



Can't blame 'em though. A blow-by-blow of the Bully's last fight'd be enough to turn any terminal chicken.

The bell sounded.

We opened with a left hook (tabbing, line and character insert/delete).

A hard right to the jaw (black characters on white background, upper and lower case character display).

A quick left jab (protected formatting, graphics, and function keys).

Then, the old uppercut (2 peripheral ports, current loop as well as EIA interface).

The ref wanted to stop the fight. But the Bully landed a roundhouse punch ($2800 price tag with OEM discounts of over 30%) that made the decision unnecessary.

The winnah and still champeen, ADDS Consul 980, the Bully!

Call me, the Bully's manager, at (516) 231-5400.

Or write Applied Digital Data Systems, 100 Marcus Blvd., Hauppauge, N.Y.

ADDS

65% of Analytical Instrument Sales in 1982 Will Incorporate μPs

The advent of the microprocessor will "completely revolutionize" the analytical instrument industry by the start of the next decade, according to findings by Darling & Alsobrook, 1801 Ave of the Stars, Los Angeles, CA 90067, based on a multi-client microprocessor consulting program. "By 1982, the U. S. analytical instrument industry will reach the $1.32 billion level—over two and one-half times that of 1975." In particular, "$858 million, or 65% of the total market will consist of instruments incorporating microprocessors."

The trend in equipment redesigns for the immediate future will be directed toward the special-purpose or functional instrument, highly automated with microprocessors and designed to meet a heavy duty-cycle or continuous operation demand with uptime well exceeding 90%. In the process control area, the study says, closed-loop monitoring is being extended to control of entire processes.

Error rates will be decreased when use of the microprocessor is extended to automatic calibration and standardization, and eventually into artificial test and diagnostic troubleshooting routines. In some applications, the study predicts, using a microprocessor within the instrument to calculate and automatically apply error correction will be much less costly than schemes for controlling those parameters.

12-Bit CMOS μP Prices Now Competitive with 8-Bit

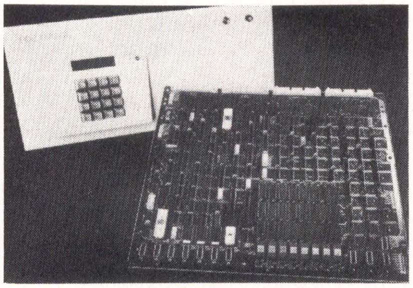
The IM6100, a complementary metal-oxide semiconductor (CMOS), 12-bit, single-chip, industrial-grade microprocessor from Intersil, Inc, 10900 N Tantau Ave, Cupertino, CA 95014, has been reduced in price from $395 to $150 in 1- to 24-piece quantities. In addition, the IM6508, a 1024 x 1 CMOS random-access memory designed to interface directly with the -6100 for use in CMOS microprocessor systems, has been lowered from $28 to $17.90 in 100-999 quantities.

Circle 175 on Inquiry Card

One-Board μComputer Has Wide Area of Application

Designed by Applied Data Communications, 1509 E McFadden Ave, Santa Ana, CA 92705 for communications systems, test applications, process controls, monitoring, data acquisition, and dedicated read-only memory (ROM)-operated device controllers, series 70, based on an Intel 8080 microprocessor, is a complete general-purpose microcomputer implemented on a 15.5 x 16-in. printed-circuit board. The system offers 4 kilobytes expandable to 16 kilobytes of random-access memory and 1 kilobyte expandable to 4 kilobytes of reprogrammable ROM.

Terminal communication is provided for teletypewriter, CRT, or modem through an asynchronous in-



put/output (I/O) with speed-select from 110 to 9600 baud, while peripheral communications is via two flat ribbon cables. Both direct memory access (DMA) and non-DMA device controllers are accommodated.

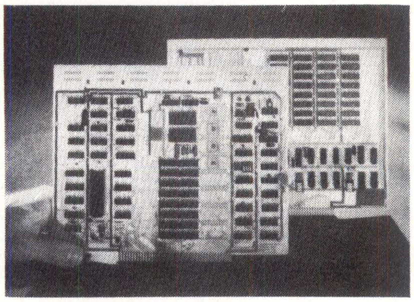
Available as options are a front-panel console, IBM-compatible floppy disc for interfacing up to eight drives, a tape cartridge, programmable real-time clock, line and character printers, 7- or 9-track magnetic tape, synchronous/asynchronous communications, general-purpose I/O card, and ROM programmer.

Software operation is 8080 compatible. Micro Executive, which permits user program development on the disc, also includes program debug, assembler, and editor on the disc.

Circle 176 on Inquiry Card

μComputer Has ROM, p/ROM, and Processor on Single PC Card

For OEM use in control, data acquisition, and data processing systems, MLP-8080 is based on an Intel 8080 type microprocessor chip. Using the system necessitates only connection



of power supplies and a serial input/output device.

The 8½ x 10½-in. (23 x 27-cm) card, introduced by Heurikon Corp, 700 W Badger Rd, Madison, WI 53713, contains space for 2048 words of static random-access memory and 2048 words of programmable read-only memory. Up to 65,000 words of memory may be addressed.

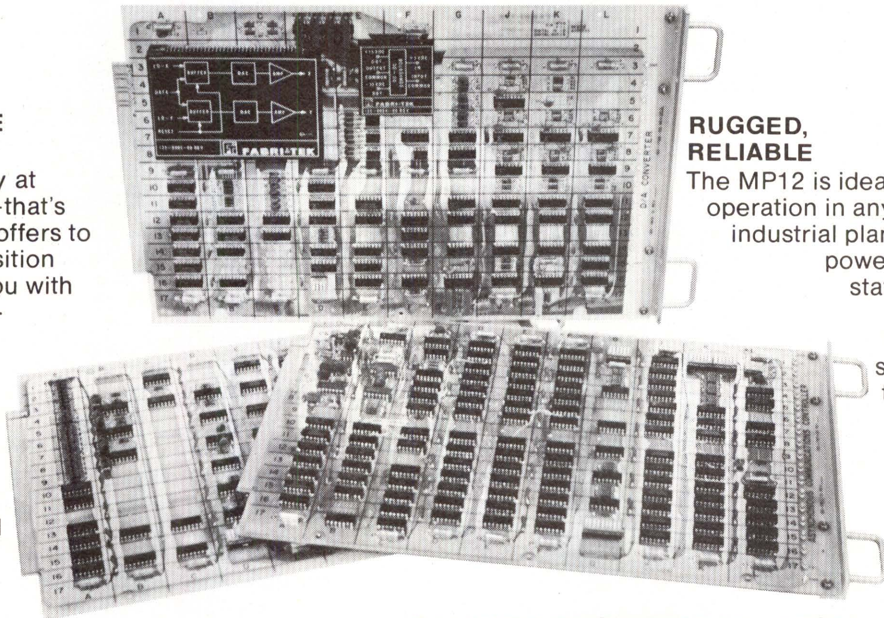
Other features include an asynchronous serial receiver/transmitter for communication with teletypewriters and CRT terminal systems. An on-card clock allows transmission rates between 110 and 9600 baud. Interfaces include a 20-mA optically isolated current loop and RS-232-C for use with modems or other devices using EIA levels. The card also contains an 8-level vectored priority interrupt system and logic for direct memory access channel control.

The MLP-8010 memory card is a 4K-word version for applications requiring larger memory capacities.

Available for system design are chassis, power supplies, and bus cards. Microcomputer-support software consists of a macro-assembler, text editor, monitor system, and an online program debugging system which includes an execution trace feature and program breakpoint capability.

Circle 177 on Inquiry Card

The MP12: for data acquisition systems with minicomputer requirements ...and a microcomputer budget.

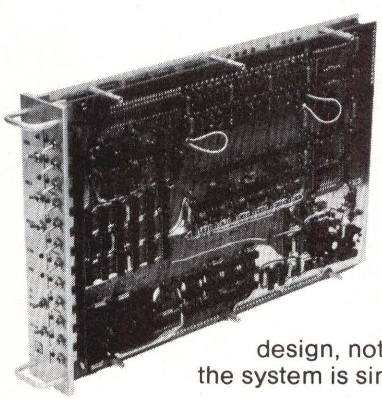


THE COST-EFFECTIVE SOLUTION

Minicomputer capability at microcomputer prices—that's what Fabri-Tek's MP12 offers to designers of data acquisition systems. We'll supply you with a complete set of ready-to-go components—CPU, software, memory, I/O controllers and subsystems—that can handle any sensor-based application. The MP12 is capable, affordable, and available . . . in 30 days or less.

RUGGED, RELIABLE

The MP12 is ideal for unattended operation in any environment—industrial plants, laboratories, power stations, pump stations, and many more! Rugged construction, no special air conditioning or power requirements.



NO HIDDEN HARDWARE COSTS

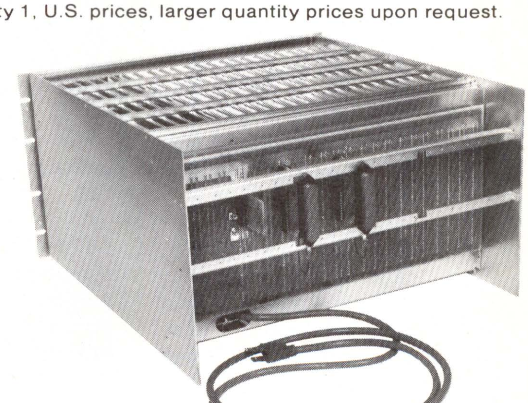
With the MP12 you eliminate the hidden development and design costs of trying to make a microprocessor do a minicomputer's job. Standard plug-in interface cards allow you to concentrate on systems design, not logic design. Expanding the system is simply a matter of plugging in additional PC cards.

COMPARE PRICE, PERFORMANCE

When you consider how much computer capability you get, the MP12 is the best bargain around. For example:

4K CPU with complete software	$1340*
Magnetic Tape Controller	$866
Digital Input Interface, 24 lines	$290
Digital Output Interface, 24 lines	$242
A/D Converter, 16 channel, 12 bit	$1386
D/A Converter, dual channel, 12 bit	$743
Asynchronous Communications Controller	$533

*Quantity 1, U.S. prices, larger quantity prices upon request.



SOFTWARE INCLUDED

No need to develop basic software—it's included in the CPU price. The RTX12 Real-time Operating System supports all commonly used data acquisition peripherals, so you can easily develop application programs. This standard package also includes diagnostics, assembler, debug and utility routines.

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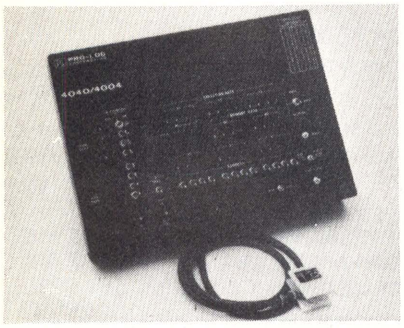
	Chicago (312)437-4116	Denver (303)753-0631	New Jersey (201)222-6250	Minneapolis (612)935-8811	United Kingdom Maidenhead 37321-4	

Portable Analyzers Test Program/Hardware in μProcessor-Based Systems

A series of portable analyzers now being delivered by Pro-Log Corp, 852 Airport Rd, Monterey, CA 93940, intended for designing and testing both program and hardware in systems using Intel 4004, 4040, 8008, 8080 or Motorola 6800 microprocessors, is said to eliminate the need for control panels, diagnostic routines, or other data processing tools.

Used in conjunction with standard oscilloscopes, they can test program and hardware either together or individually. The analyzers display all data related to a selected instruction cycle and generate a scope sync pulse. They interface to the system under test through use of a dual-inline package connector (on a 3-ft cable) that clips onto the microprocessor.

Systems may be tested in either a static, single-step mode, whereby

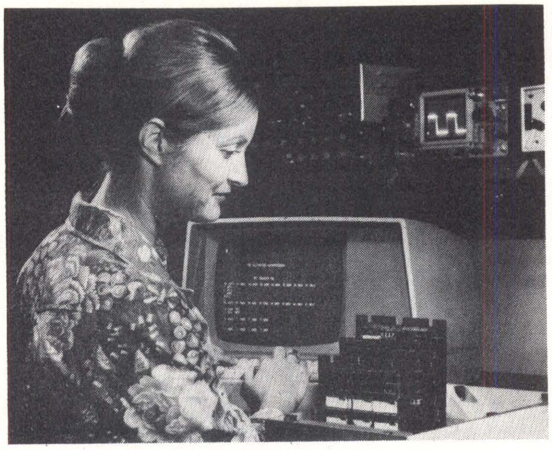


the program is stepped through each memory cycle, or in dynamic run mode, in which data for a full instruction cycle are captured and displayed while the program is in operation.

The self-powered analyzers operate on a standard 115-Vac voltage supply, and automatically reference to the most positive supply voltage on the microprocessor being tested. They are supplied in aluminum cases and weigh approximately 4.5 lb.

Circle 178 on Inquiry Card

Mil-Qualified μComputer Built with Commercial μProcessor Chips



Microcomputer built with 16 2-bit bipolar Schottky LSI circuits (white rectangles) is in final testing at Hughes Aircraft Co. The fully militarized unit, packaged onto three 5.6 x 6.2-in. cards, offers 500,000 operations/s with up to 64K words of memory

A 16-bit microcomputer, constructed with commercially available, large-scale integration (LSI) microprocessor chips providing the speed and flexibility for military applications, is being tested at Hughes Aircraft Co, Data Systems Div, Culver City, CA 90230 as part of its Navy digital missile autopilot research and development program.

Featuring military temperature-range capabilities and 500,000 operations/s—10 times greater than recent state-of-the-art minicomputers, according to division manager William Shockency, MMC consists of eight 2-bit commercial bipolar Schottky LSI circuits for performing arithmetic functions; and one 2-bit LSI control chip, four programmable read-only memories, and 48 medium-scale integrated components making up the memory and control functions.

The 50 instructions most useful for avionics and military systems work for MMC were selected, and seven addressing modes for flexible access to the processor's up to 64K words of memory are provided. Typical instruction times are: addition/subtraction, 1.2 μs; load, 1.5 μs; store, 2 μs; jump, 1.75 μs; and multiply, 10.5 μs. Also provided for efficient programming are eight registers, organized as two index registers, four accumulators, stack pointer, and program counter.

With respect to support software, an assembler simulator, and a microprogram translator for the MMC are currently available on several commercial computers, including the IBM System/370 and Xerox Sigma 5 and 9.

The Air Force Avionics Laboratory at Wright-Patterson Air Force Base is using the MMC in its modular digital scan converter; mobile ground and helicopter fire control systems, coordinate converters, and other distributed processor systems are also possible applications. Preproduction evaluation units will be available next month.

Circle 179 on Inquiry Card

μP-Based Data Entry Terminal Features Visual Display

Designed for offline capture of data on magnetic tape cassettes as well as for use as a remote batch-entry device, the 7200 model I, equipped with either a keypunch or typewriter-style keyboard, incorporates a 9-in. CRT screen which displays the standard 64 ASCII character set. The top half of the screen accommodates 128 characters; the lower half is for operator or system status messages. Operating modes include data entry, data verify, search, format entry, format verify, format display, transmit batch, and receive batch.

Announced by NCR Corp, Dayton, OH 45479, the terminal is based on a single-chip microprocessor which features a 5-μs instruction cycle time, four addressing modes, and 78 hardware commands. The microprocessor and associated read-only and random-access memories direct all buffer allocation, data formatting, and input/output traffic between the terminal and its peripherals. Error interception, operator guidance, and data verification are also provided.

Data cassettes used are ANSI compatible, can be read into the company's full line of computer systems, and store over 300,000 characters each. Recording density is 800 bits/in.

Circle 180 on Inquiry Card

Compiler Facilitates µComputer Programming

Used in conjunction with PCL (process control language)—a high level language designed for programming programmable read-only memories, the Process Control Compiler from The Warner & Swasey Co, Comstar Microcomputers Electronic Products Div, 30300 Solon Industrial Pkwy, Solon, OH 44139 handles the instruction sets for the company's systems 4A and 4B microcomputers, built around the Intel 4040 microprocessor chip. The unit allows data to be entered from data terminals;

in addition, eight commands devised specifically for compilation from a terminal permit such functions as creation on tape of an entire PCL program or adjustment of the amount of delay following a carriage return.

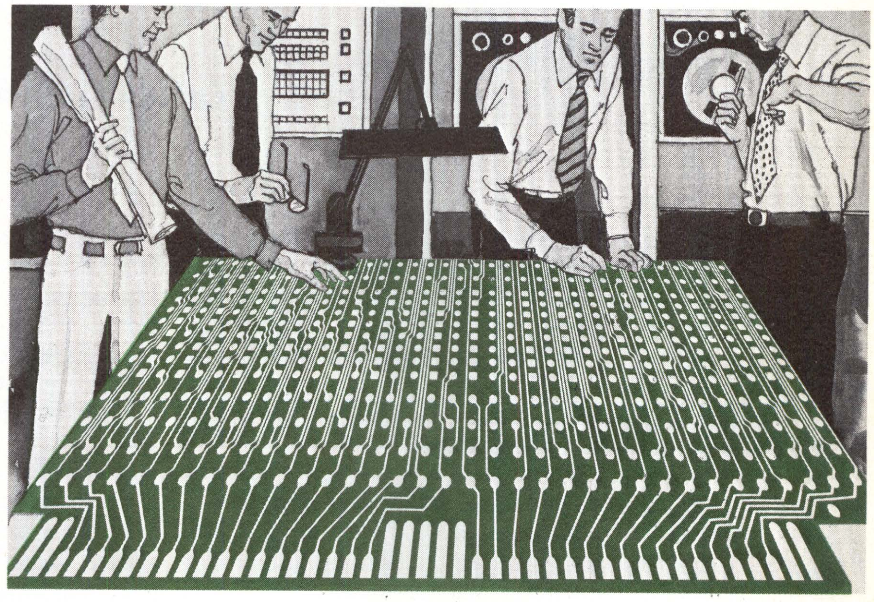
Circle 181 on Inquiry Card

µProcessor System Design Employs n-Channel Ion-Implantation

Series 1600, announced by General Instrument Corp, Microelectronics Div, 600 W John St, Hicksville, NY 11802, is based on a 16-bit microprocessor chip constructed using the company's n-channel ion-implant Giant II process. The design incorporates eight 16-bit general-purpose registers, all of which are program accessible and can be used as accumulators or address registers. Six can be used by the running program; one is used as the memory stack pointer providing last-in/first-out storage in the main memory, the eighth as the program counter. General registers and the high speed pipelined arithmetic/logic unit and its status register form the data processing logic.

N-channel MOS/LSI logic devices include read-only and random-access memory circuits. An intelligent input/output interface capability is complemented by programmable interface controllers. Compatible assembler/simulator software is available for popular minicomputer systems and large time-sharing systems. Comprehensive subroutine libraries, diagnostics, utility programs, and an online debug program are also available. In addition, a language generation program enables development of a high level language to match each application.

Circle 182 on Inquiry Card



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CIRCLE 58 ON INQUIRY CARD

PRODUCT FEATURE

Portable Computer Combines Microprocessor Technology with Large-Computer Performance

Intended for standalone computing chores in scientific, engineering, or business facilities, the model 5100 Portable Computer enables on-site analysis of data or solution of quantitative problems without the need to time-share larger computers. Slightly larger than an IBM typewriter and weighing about 50 lb, the desktop unit, announced by International Business Machine Corp's General Systems Div, has the computing capacity of a small System/360 but is based on a microprocessor.

Standard features include combination keyboard for data entry and commands, CRT display, processing unit with up to 64 kilobytes of main memory, tape cartridge for storing programs, and adapter for attaching external black and white TV monitors. Adding an optional communications adapter permits use as a communications terminal to remote System/370 computers. Depending on model, APL and/or BASIC languages are used for programming and operation.

Components

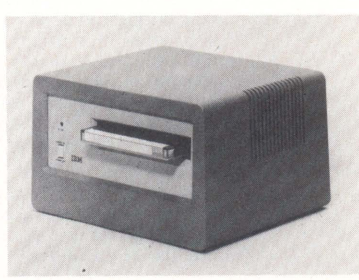
Overall system and data flow control is provided by a single-card microprocessor that contains registers and an input/output (I/O) channel. Language implementation is made in read-only storage (ROS).

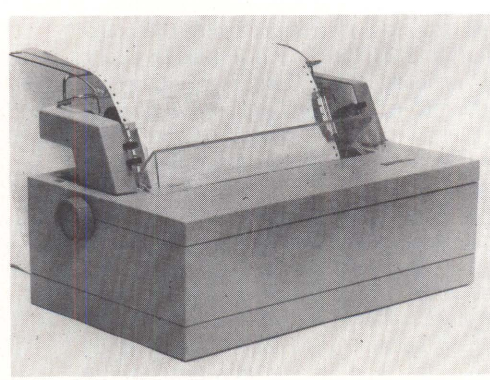
A basic unit contains 16 kilobytes of read/write (R/W) or main storage for user work space, but up to three more 16-kilobyte increments may be included. Twelve models of the 5100 are available: A1 through A4 operate with APL, B1 through B4 operate with BASIC, and C1 through C4 use APL and BASIC. (1 through 4 indicate number of 16-kilobyte increments of R/W storage included.)

Internal processor average microinstruction time is 1.75 μs. Storage access time is 354 ns and cycle time is 530 ns. Circuit density of each MOSFET technology ROS chip is 48 kilobits. (Chip size is approximately 0.23 in. sq.) Up to 190 kilobytes of ROS may be included. R/W storage is 8 kilobytes per circuit card (two cards per 16-kilobyte increment).

Typewriter-style keyboards are in three configurations to match the language(s) to be used. (Model C has dual-function keys.) A calculator pad on the same panel contains 10 numeric, one decimal, and four arithmetic function keys. An Execute key is common to both sets of keys. Sideways movement of the cursor and up and down scrolling of lines are controlled by display keys. Commands are entered by holding down one of 14 program command keys and pressing the appropriate function key. The numeric keys, for BASIC, can be used to initiate and perform special functions that the user has programmed and stored. Other keys provide capabilities such as copying the CRT display on an optional printer.

A 1024-character CRT screen, organized in 16 lines of 64 characters each, provides a display of data keyed in as either black on white





Optional equipment. Auxiliary tape unit extends user's workspace; it uses same tape cartridge as computer. Matrix printer provides hard copy, serially left or right, at 80 char/s from either commands in the user's program or when a computer function key is pressed or white on black. Users can edit inputs before they are entered into the system or before they are printed. When large amounts of data are on the screen, blanks can be inserted between display characters to separate the left or right 32 and make them easier to read. All special APL and BASIC characters can be displayed.

A 3M-type data cartridge (full-size configuration) serves as a removable medium for data and program storage. Up to 204,000 characters of data can be stored on its 300 ft of 1/4-in. tape. The data cartridge unit operates at 40 in./s in read, write, search, and rewind modes, yielding an effective read rate of 2850 char/s and a write speed with checking of 950 char/s. Each tape contains a file protect feature.

For systems requiring hard copy records or which have large file sizes, an optional external I/O adapter allows ready connect or disconnect of a matrix printer and/or an auxiliary tape unit. Hardcopy output can be provided by the optional 80-char/s, 132-print position matrix printer on single sheets, multiple copies, or multi-part paper. The model 5103 prints serially from both left to right and right to left, at 10 char/in. with 6-line/in. vertical line spacing. Print commands may originate in the user's program or from a keyboard function key. All or part of the information on the screen will be printed as determined by the user. Printer dimensions are 12 1/4 x 13 1/4 x 23" (31 x 34 x 59 cm); weight is 60 lb (28 kg).

The model 5106 auxiliary tape unit is an optional device for users who have extensive copy requirements or file sizes which exceed standard work space. Characteristics are the same as those of the data cartridge unit in the computer. The same cartridges can be used in both units. Size of the auxiliary tape unit is 7 1/4 x 10 x 12 1/4" (19 x 26 x 31 cm); weight is 18 lb (8.2 kg).

When the computer is used in communications mode as a terminal, it can communicate with most System/370's that support the IBM 2741 (start/stop) mode with extended binary code decimal (EBCD). With optional printer attached, standard 2741 printing capability is attained. The tape cartridge may be used to transmit and receive messages.

Other Features

Installation of this computer consists of unpacking, plugging it into a grounded 115-Vac outlet, and checking it for proper operation through a series of tests described in the reference manual. The unit can be moved from office to office, rather than requiring users to bring their work materials to it. An optional carrying case with hand and shoulder straps provides environmental protection if the computer must be moved to another building or site.

Three optional Problem Solver Libraries are available in tape cartridges: mathematical problems (37 APL and 44 BASIC), statistical techniques (40 APL and 41 BASIC), and business analyses (30 BASIC). Each library contains frequently used interactive routines or functions. Capabilities for the three libraries include, respectively, solution of linear equations, eigenproblems for real matrices, and integration of first-order differential equations; data generation, elementary statistics, and regression and correlation; and cost studies, resource projections, and product profitability analyses.

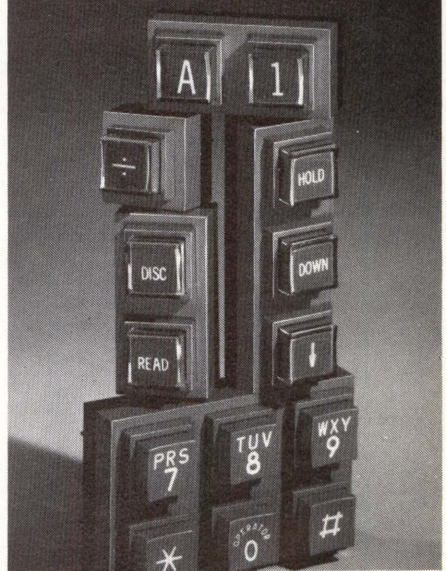
To use a library, the user loads the proper cartridge and activates the tape cartridge unit. As the routines are displayed on the screen, the user selects the individual routines he wishes to run, and the computer then prompts and guides him through to completion of the problem.

Price and Delivery

All models of the 5100 Portable Computer are available only on a purchase basis. Prices range from $8975 to $19,975, depending on language and amount of memory desired. The model 5103 printer sells for $3675, and the model 5106 auxiliary tape unit is $2300. Each Problem Solver Library, consisting of two tape cartridges and a user's guide, is available for a 1-time monthly charge of $500. All units are customer-installed. Maintenance is available on either contract or per call, time and material service. Delivery is three weeks ARO. International Business Machines Corp, General Systems Div, PO Box 2150, Atlanta, GA 30301. Tel: (404) 256-6799.

For additional information circle 199 on inquiry card.

Grayhill coded output switch modules stack up!



new performance standards...
1,500,000 cycles with less than 10 milliseconds bounce

- Self-generated logic...7 wire coding capability
- Can be stacked in any array
- Telephone array will provide standard frequency selection

This "second generation" of low-profile Grayhill pc mountable push-button switch modules passes exacting test for life and for bounce. Choose 6-, 3-, 2- and 1-button horizontal or vertical modules, to array in any format, including telephone key set, while maintaining constant center-to-center spacing! Circuitry available as SPST through 4 PST, normally open, or the poles can be internally shorted so several terminals connect when button is actuated. Choice of colors, with hot stamped or molded-in legends. For more information on these Series 82 modules, consult EEM or ask Grayhill for engineering data.

Grayhill INC.

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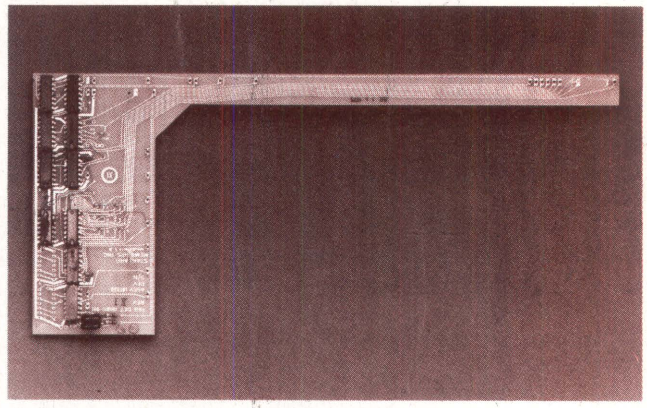
CIRCLE 59 ON INQUIRY CARD

PRODUCTS

Extended Memory Unit Expands Nova 2/10 Capability to 80K Words

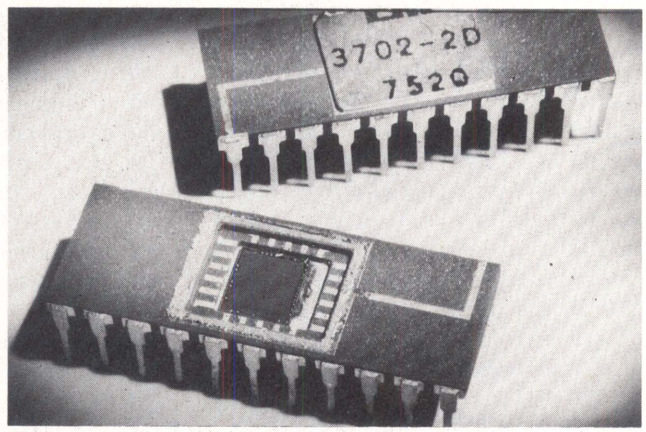
Addition of the EMMU, or extended memory mapping unit, allows users of Data General Corp Nova 2/10 processors to expand maximum addressable memory from 32K to 80K words without modifying the CPU. The unit is configured as a single PC board containing TTL mapping, device address patch, and base memory size patch. It plugs directly onto the wirewrap side of the processor's backplane, without obstructing access to the backplane for I/O cabling. Base memory may be either 8K or 16K, with up to four 16K extension core memory modules added as contiguous address space. Selection of extension memories as augmentation is user programmable. The EMMU maps only the extension memory modules. Memory mapping and validity checking are performed on each memory cycle, with no increase in memory access time. **Standard Memories, Inc,** 2801 E Oakland Park Blvd, Fort Lauderdale, FL 33306.



Circle 200 on Inquiry Card

Ultra-Fast 2K n-MOS Static RAMs To Compete with Bipolar Memories

Designed as replacements for smaller capacity bipolar and static MOS RAMs, the 3702-1 and -2 are claimed to be the first 2-kilobit n-channel MOS static RAMs to compete favorably with those devices in price and speed for large capacity, high speed memory applications. Organization is 2048 words x 1 bit. A fully static memory cell eliminates the need for refresh or charge-pump circuitry. Access times are 90 and 70 ns max, respectively, for the -1 and -2. Read and write times for both are 188 ns min. Typical power dissipation (at 70°C ambient) is 225 μW/bit operating, 45 μW/bit standby. Other features include on-chip address input latches, low voltage inputs (except Chip Select), differential output sink current and OR-tie capability. Packaging is standard 22-pin DIL. Chip Select simplifies memory expansion. Chip Select time is 88 ns min, 500 ns max. Op temp range is 0 to 70°C; storage temp range is −55 to 125°C. **Cambridge Memories, Inc,** 12 Crosby Dr, Bedford, MA 01730.



Circle 201 on Inquiry Card

Modular Video Display Terminal Permits System Designer to Choose Component Location

The ADM-2 is packaged such that each of three elements—CRT display, keyboard, and control circuitry/power supply components—can be placed where it can be used most efficiently. The flicker-free CRT displays full u/lc ASCII 128-char set in a 24-line, 80-char/line format; 1920 char can appear on the 9" screen at one time. A 4" high keyboard module contains 63 alphanumeric keys in typewriter format, 10-key numeric pad, 16 function keys to execute 32 standard commands, cursor control (separately located), and four transmission control keys. The operator can clear the screen, change characters, and insert or delete characters or lines. Total cursor control permits the user to skip, backspace, forespace, move up or down, return, home, and originate a new line. Part of the display can be held in protected field at a low light level; after new data are entered in the unprotected field and viewed, only those data are transmitted to the computer. Asynchronous transmission is panel selectable at rates of 110, 150, 300, 600, 1200, 2400, 4800, or 9600 baud, in half- or full-duplex modes. **Lear Siegler, Inc, Electronic Instrumentation Div,** 714 N Brookhurst St, Anaheim, CA 92803.

Circle 202 on Inquiry Card

Just a few letters of recommendation

They spell out the 1602's (AN/UYK-19) qualifications to provide computer power for tough jobs. Rolm computers are at work today on land, sea and in the air.

Not only does the AN/UYK-19 meet Mil Specs, it offers a microprogrammable processor with 200 nanosecond cycle time and provision for four-fold expansion of microcode. Dual port core memory up to 256K along with high speed semiconductor memory and various read only memory options gives unlimited flexibility. Vectored I/O and stack processing make programming real time applications easier and help reduce overhead.

At no added cost, we provide the most extensive software package available with a military computer —proven in over 10,000 installations. Plus there's documentation, extensive training, and fast delivery. End result—letter perfect computers for rugged applications.

Call (408) 257-6440, TWX 910-338-0247 or write Rolm Corporation, 18922 Forge Drive, Cupertino, CA 95014. In Europe: 06181 15011, TWX 841-418-4170, 645 Hanau, Muehlstrasse 19, Germany.

ROLM CORPORATION

The Rugged Computer Company

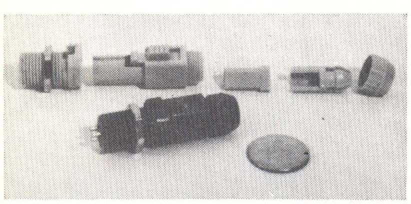
DATA LINK SIMULATOR

Primary function of the DLS106 is to provide a means of evaluating performance of digital terminal equipment in a noisy transmission environment without field testing. It generates error burst rates from 1 x 10^{-9} to 0.5 (total error) and errors per burst from 0 to 999. Heart of the unit consists of feedback shift registers which generate max length, pseudorandom binary sequences. Register outputs are combined to generate a statistically random error signal. The simulator operates at data rates to 10 MHz. **General Data Products, Inc,** PO Box 159, Willow Grove, PA 19090.
Circle 203 on Inquiry Card

HEAT EXCHANGER

The Z-duct electronics cooler, an air-to-air heat exchanger that makes hermetic sealing of electronics enclosures economically feasible when cooling with air, is a simple counterflow device. Consisting of a folded heat transfer surface, fitted within a duct so as to divide it into separate yet intermeshed passages, it permits opposing air streams to be brought into close proximity while cross-contamination is prevented. **DesChamps Laboratories Inc,** 8 Great Meadow Lane, East Hanover, NJ 07936.
Circle 204 on Inquiry Card

PLASTIC, CIRCULAR CONNECTOR

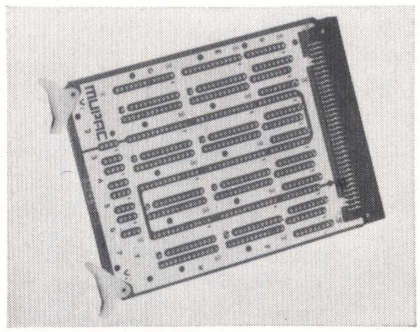


Series D 3-pin, all plastic, quick disconnect connector features include low cost, no shock hazard, elimination of ground lead for case, and retention of appearance after rough handling and abrasion. Contacts are brass; plating is 10-μm gold over 300-μm silver. Life is rated at >100,000 cycles and resistance is <5 mΩ. The units have 3-A current rating and a 5- to 2.5-oz insertion force. Male or female contacts are available in either plug or receptacle. **Hypertronics Corp,** 154 Great Rd, Stow, MA 01775.
Circle 205 on Inquiry Card

FLOPPY DISC TESTER

Testette model 33 FD tests for modulation, missing pulse, and extra pulse, with a throughput time of 1, 1.6, or 3.2 min., depending on degree of surface testing desired and whether or not track overlap testing is required. Tests are made at singular, adjustable analog clipping levels and performed over 234 tracks. In production test mode, when an error is encountered, the certifier aborts the test automatically, returns the carriage to home, and indicates on the front panel the type of error detected. **Three Phoenix Co,** 10632 N 21st Ave, Phoenix, AZ 85029.
Circle 206 on Inquiry Card

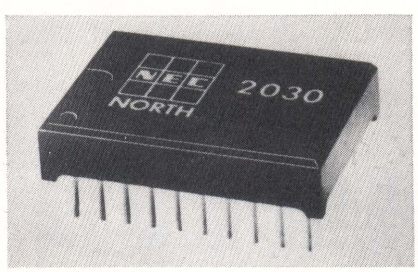
MICROPROCESSOR PANELS



Family of 3-potential (V1, V2, gnd) wire-wrapping panels is designed for use with current 18- to 40-pin microprocessors. Panels accept RAMs, ROMs, and microprocessors with different package pin-counts and spacing, voltage requirements, and system operation, as well as eight or 10 different speed or power options. A complete line of complementary hardware and 3-potential connector backplanes and rack assemblies are also available. **Mupac Corp,** 646 Summer St, Brockton, MA 02402.
Circle 207 on Inquiry Card

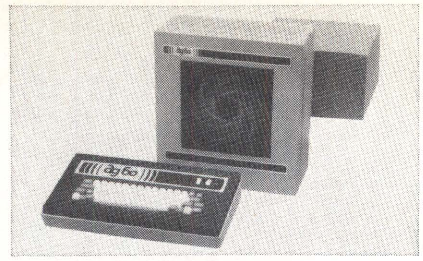
CONTROLLER FOR STEPPING MOTORS

Type 2030 includes TTL control logic, pre-driver transistor circuitry, and diodes to protect against inductive transients. Each of four outputs delivers 40 mA min and operates with motor supply voltages of 40 Vdc or less. The unit controls bidirectional motors and operates 1 of 3, 1 of 4, or 2 of 4ϕ motors. **NEC Microsystems,** 1150 NW 70th St, Fort Lauderdale, FL 33309.



Circle 208 on Inquiry Card

GRAPHICS DISPLAY TERMINAL

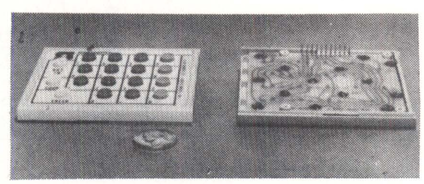


Incorporating a building-block approach that allows users to buy only necessary features, the AG 60 uses a 512 x 512 line plasma display panel, with 60-line/in. resolution. Features include a second, independent char generator to permit display of two sizes of characters on the same screen, programmable matrix generator for definition and display of 64 independent 8 x 16 dot matrices at any location on the panel. Unrestricted matrix format allows display of alphanumeric char at any location on the panel. **Applications Group, Inc,** PO Box 444, Maumee, OH 43537.
Circle 209 on Inquiry Card

PROGRAMMABLE COMMUNICATIONS PROCESSOR

Model 1380 is a functional replacement for the IBM 270X and 370X communications controllers, attaching directly to a System/360 (models 30 and above) byte multiplexer channel and/or to a System/370 (model 135 and above) selector, byte, or block multiplexer channel. Aggregate data rate is 100 kilobytes/s. Featuring diagnostic and dynamic line switching, the processor also offers expansion capabilities plus expandable MOS memory, and supports a wide variety of non-IBM terminals. **Memorex Corp,** San Tomas at Central Expy, Santa Clara, CA 95052.
Circle 210 on Inquiry Card

LOW PROFILE KEYBOARD FOR DATA ENTRY



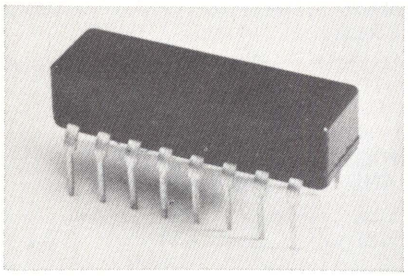
Designed for digital entry applications, this keyboard mounts flush to the panel face. Depth behind panel face is 0.38"; key buttons extend 0.22" above panel face. Available in std single-key button, 10- and 12-station configuration, the keyboard offers 5 million-operation life, customized legend dress bezel, non-teasable contact, and ease of mounting independent of panel thickness. Lighted buttons are available using LEDs in each. It provides spst momentary action and 15-Vdc max with MOS, TTL, and DTL compatibility. **Stacoswitch, Inc,** 1139 Baker St, Costa Mesa, CA 92626.
Circle 211 on Inquiry Card

LED SCANNER

An LED reflective scanner which can detect white bond paper from up to 10" away without requiring pulsed electronics, the S20001 Max-Coax can be used with a 1"-dia retroreflector at distances of 100" without pulsed electronics. The scanner consists of a specially selected LED and matched silicon phototransistor. IR energy from the LED is reflected from the target back to the phototransistor through a blocking filter and gathering lens system. The filter completely blocks out all visible light and attenuates most radiation from fluorescent lamps. **Skan-A-Matic Corp,** Rte 5 West, Elbridge, NY 13060.

Circle 212 on Inquiry Card

WIDEBAND OPERATIONAL AMPLIFIER



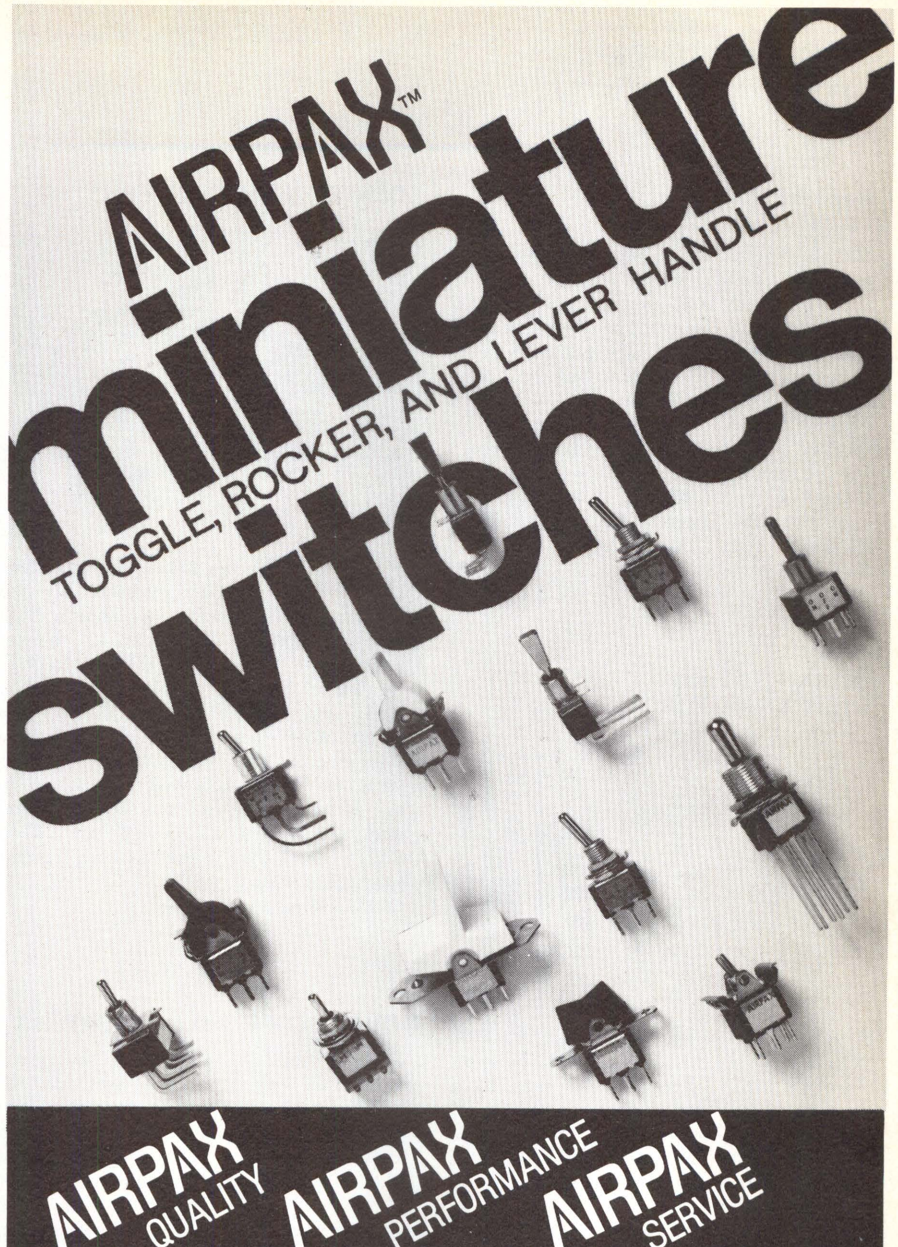
Model 9916 provides a conveniently packaged op amp having closed-loop bandwidth capability exceeding 100 MHz and uniform 6-dB/octave rolloff rate providing good high-frequency stability. Supplied in a std 14-pin DIP, it features 150-MHz min guaranteed gain bandwidth product, 60-dB open-loop gain at dc, and ±300 V/μs min slewing rate. **Optical Electronics, Inc,** PO Box 11140, Tucson, AZ 85734.

Circle 213 on Inquiry Card

FLATBED PLOTTER

Featuring interchangeable heads and removable panels that adapt the equipment for either line or photo plotting in <3 min., the AP53 graphic plotter has a 10-in./s speed during painting, up to 40 in./s when line plotting, and can output 33 x 45" drawings on either conventional or photosensitive media. Its aperture plane contains up to 144 apertures on four changeable plates and the fiber optic bundle can be rotated 180 deg in increments of 1 deg. Positioning accuracy is 1 mil/ft/axis; overall accuracy is 5 mils. **Applicon Inc,** 154 Middlesex Tpk, Burlington, MA 01803.

Circle 214 on Inquiry Card



American made. Competitively priced. Airpax miniature switches are the product of years of experience in the design and manufacture of electromechanical devices.

Single and two pole models. Maintaining or momentary switching actions. A wide range of options for appliances, industrial, military, and consumer applications.

You can choose the exact combination required from the selection of basic switching functions, contact ratings, terminations, handle types, and hardware.

Airpax miniature switches assure you of the superior quality, performance, and service that has been synonymous with Airpax products throughout the years.

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AMERICAN DATA, Huntsville, Alabama – *TV Products*

CIRCLE 61 ON INQUIRY CARD

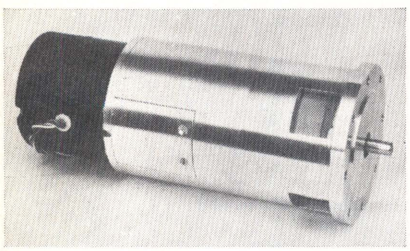
PRODUCTS

HALL-EFFECT DIGITAL SWITCHES

ULN-3006T is a magnetically operated solid-state switch with a digital current-sinking output, with no electrical contacts to cause noise, bounce, or contamination. The "T" pack interfaces directly with most electronic circuits' discrete transistor circuits, IC logic, and SCR. No buffer circuitry or amps are normally required. Integrated on the chip are Hall sensor, voltage regulator, Schmitt trigger, and amp. Operating speeds of 100 kHz are attainable. **Sprague Electric Co,** 555 Marshall St, North Adams, MA 01247.

Circle 215 on Inquiry Card

INTERPOLATING STEPPER MOTOR



Producing 1.8-deg steps at rates to 20,000/s, the IS-50K-150 provides for interpolation between the 1.8-deg step positions to a resolution of 0.18 deg. Since interpolation takes place at the same time the motor is making the step, it does not slow the operation. Stepping rate in interpolating mode is 50,000 0.18-deg steps/s; 5000/s in 1.8-deg mode and 6000/s in 0.18-deg mode. Torque capacity is 150 oz-in. with stiffness of 15 oz-in. at 0.18 deg. The interpolator prefers inertial or low friction load and provides accuracies of ±0.18 deg. **Mesur-Matic Electronics Corp,** 50 Grove St, Salem, MA 01970.

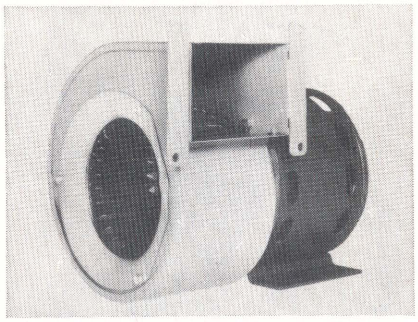
Circle 216 on Inquiry Card

NON-ILLUMINATED PUSHBUTTON SWITCHES

Unipush switches feature concave faces as well as momentary and push-lock/push-release. Five series provide a variety of non-illuminated pushbuttons, switching, terminal, and mounting methods including PC. Series PB11 are 23/32" sq for ¾" (min) mounting centers, series PB12 are 31/32" sq for 1" (min) centers. Series UP-100/-200/-500 and UP-400/-800 are designed for front/rear-of-panel mounting, respectively. Contacts are welded crossbar gold alloy; contact rating is dry circuit to 1 A. **Switchcraft, Inc,** 5555 N Elston Ave, Chicago, IL 60630.

Circle 217 on Inquiry Card

CENTRIFUGAL BLOWERS



SC series covers the wheel dia range from 1½ to 5¼" and zero-pressure air flow rates from 6 to 245 cfm. Available in clockwise or counterclockwise rotation, blowers consist of a centrifugal-type impeller, scroll-type housing of plastic or painted steel, and shaded-pole or split-capacitor motor. Motors have Class A insulation and sleeve or ball bearings, and are equipped with either UL-approved impedance-type or thermal overload protection. Overall sizes range from 3.73 x 2.87 x 3.58" to 8.52 x 8.27 x 7.83". **Torin Corp,** Torrington, CT 06790.

Circle 218 on Inquiry Card

DUAL-SLOPE A-D CONVERTERS

ADC-EP series high resolution, ratiometric dual-slope converters are available with 14-binary bit or 4½-BCD digit resolution. Both have sign-magnitude coding. Analog input is floated by means of optical isolation and transformer coupling to give ±300-V common mode capability with 100-dB common mode rejection. Conversion time is 230 or 260 ms. Gain tempco is ±8 ppm/°C max for the internal reference, and ±5 ppm/°C for the converter. Zero drift is stabilized by an automatic zeroing circuit to ±1 μV/°C max. **Datel Systems, Inc,** 1020 Turnpike St, Canton, MA 02021.

Circle 219 on Inquiry Card

10-BIT A-D CONVERTER

Model 2800, a successive-approximation ADC, requires 1 μs max to complete a 10-bit conversion. Housed in a 2 x 4 x 0.375" electrically and magnetically shielded module, the unit features throughput rates to 1 MHz and typ differential nonlinearity of ±¼ LSB. Max coefficient of gain is ±10 ppm/°C, tempco of differential nonlinearity is ±3 ppm/°C, ensuring monotonic operation over the 0 to 70°C op temp range. Input ranges are 0 to −5 V (2801), 0 to −10 V (2802), 5 to −5 V (2803), and 10 to −10 V (2804). **Dynamic Measurements Corp,** 6 Lowell Ave, Winchester, MA 01890.

Circle 220 on Inquiry Card

LOW POWER SCHOTTKY MULTIPLIER

Am25LS14 is an 8-bit x 1-bit serial/parallel 2's complement multiplier built with low power Schottky processing techniques. It takes an 8-bit multiplicand at the parallel X inputs and multiplies it by the multiplier that is clocked serially into the Y input. The 2's complement product is available at the serial output. Typ 16 x 16-bit multiplication is accomplished in approx 1 μs. Available in a molded or hermetic DIP and ceramic flat package and specified for operation over commercial and mil temp ranges, the circuit may also be used for magnitude-only multiplication. **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.

Circle 221 on Inquiry Card

HIGH VOLTAGE DIODES AND RECTIFIERS

Line includes G100 series microminiature high voltage diodes and diode banks, designed for portable image-intensifier power supplies, and G120 and G110 series high voltage rectifiers. G100 units provide 1- to 6-kV PIV voltage range; 20-mA avg current, high surge-current capability, and fast recovery. Specs for the G120 and G110 include 8- to 40-kV and 2- to 10-kV PIV voltage range and 10- to 350-mA and 10- to 125-mA avg current, respectively. **Galileo Electro-Optics Corp,** Galileo Pk, Sturbridge, MA 01518.

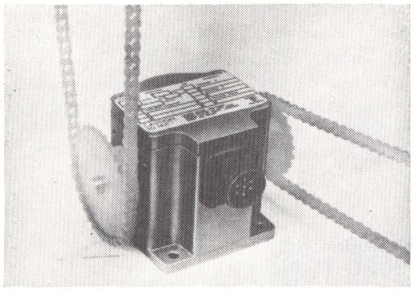
Circle 222 on Inquiry Card

PULSE GENERATOR

Providing pulse widths from 100 ns to 0.1 s and rep rates of 5 Hz to 5 MHz (±5% accuracy), the model 20 provides TTL-compatible output capable of driving ten 7400 TTL gates. Pulse generator 1 is coupled to a second pulse generator with the trailing edge of the first setting off the second. In turn, the trailing edge of the second sets off the first, thus reinitiating the cycle. Both are independently adjustable over a range of 100 ms to 100 ns in six steps with an interpolating, continuously variable potentiometer. **Advanced Electronics Corp,** 63 Lincoln St, Newton Highlands, MA 02161.

Circle 223 on Inquiry Card

ROTARY PULSE GENERATOR



TRU-Tax incremental encoder, featuring a double-ended 3/8" dia shaft supported on widely spaced, sealed bearings, withstands 100-lb radial shaft loading, allowing it to be driven by chains, belts, or gears. A heavy walled, gasketed case completes the package, which is designed for rugged industrial applications. The unit is supplied in single- or dual-channel versions, with resolution to 600 ppr, optional marker pulse and line driver, and LED light sources. **Trump-Ross Industrial Controls, div of Datametrics, Inc,** 265 Boston Rd, North Billerica, MA 01862.
Circle 224 on Inquiry Card

VOICE DATA ENTRY TERMINAL

Replacing or complementing intelligent CRT/keyboard stations by enabling the user to enter data by voice, the 500 is suited for large, multiterminal data entry systems. Only a display and a small operator console are required at each work station. The display permits visual verification of each entry and can be used interactively to guide the operator through a data entry sequence. The control console provides a microphone input connector and allows selection of employee number and mode of operation. **Threshold Technology, Inc,** 1829 Underwood Blvd, Delran, NJ 08075.
Circle 225 on Inquiry Card

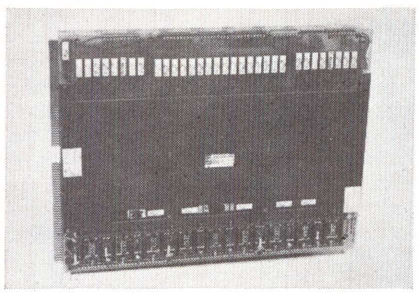
μP-CONTROLLED PUNCHED-CARD DATA ENTRY DEVICE

The 501 data entry microprocessor, incorporating an RS-232-C interface, is suited for minicomputer card input or output, is capable of data transmission via modem or cable, and can be tied into virtually any type of data entry or processing system. It reads, punches, prints, verifies, and interprets either on- or offline. Features include up to 220 col of constants from memory, up to 28 program levels with automatic sequencing, instant verification, automatic error correction, and high speed char duplication. **Tab Products Co, Data Entry Div,** 2690 Hanover St, Palo Alto, CA 94304.
Circle 226 on Inquiry Card

AC MOTORS FOR DISC DRIVES

"Thick ring" 50-, 60-, and 400-Hz induction motors for use in disc memory drives include model 300, a ruggedized, high temp unit, with 1ϕ, 115-V, 60-Hz capacitor start, capacitor run designed for a gas-pressurized disc memory system, which is supplied as an unhoused or frameless unit for mounting within a pressure-and-cooling system. The motor operates at a continuous design torque load of 50 oz-in. and exhibits max stall of 32 oz-in. using a 32-mFd capacitor. Nom design speed is 3440 rpm, corresponding to a max continuous output of 0.11 hp. **Sierracin/Magnedyne,** 5580 El Camino Real, PO Box 458, Carlsbad, CA 92008.
Circle 227 on Inquiry Card

CORE MEMORY SYSTEM



The basic 696 consists of 16,384 x 18-bit words on a single 11.75 x 15.4" module. Up to eight modules may be used in a single enclosure. The system is field-expandable to 256K words x 9; 128K words x 18; or 64K words x 36. Full cycle time is 650 ns; data access time is 250 ns. The memory is compatible with TTL logic and is a direct plug-replacement for Micro 3000 series memories. Options include enclosures with built-in expansion capability, power supplies, and extender boards. **Fabri-Tek Inc,** 5901 S County Rd 18, Minneapolis, MN 55436.
Circle 228 on Inquiry Card

DIGITAL PHASE METER

Featuring ±0.03-deg accuracy, attained using signal-conditioning circuitry and an ultra-stable reference source, model 305 provides a 5-digit-plus-sign illuminated readout of phase angle, and auxiliary BCD digital and analog phase-angle outputs on the rear panel for measurement or control system integration and recording. Angle measurements are performed over a frequency range from 1 Hz to 11 MHz. **Dranetz Engineering Laboratories Inc,** 2385 S Clinton Ave, South Plainfield, NJ 07080.
Circle 229 on Inquiry Card

INFO-LITE

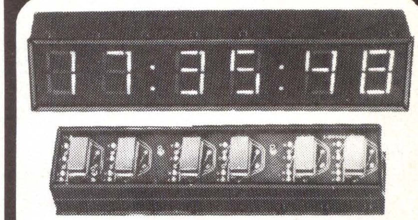
INDICATORS

MODULAR APPROACH PROVIDES CUSTOM LIGHTED INDICATORS WITH LOW INSTALLED COST

Any group of messages can be displayed in B&W or color(s) • Module sizes 3/8" sq. to 3/4 x 1 1/2 • Supplied with bezel, ready to snap into panel cutout • Uses std. T 1 3/4 lamps • Common ground reduces installation cost • Serviced from front.

CIRCLE 62 ON INQUIRY CARD

NUMERICS

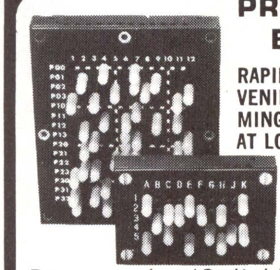


READY TO INSTALL — VIEWING TO 150 FT.

Indoor or outdoor • 7", 1", 2", 3" and 5 1/2" characters • Attractive, multi digit package includes bezel and "Black-Out" front panel • Message modules and ± indicator optional • Decoder-driver, Memory and/or Counting logic available • All wear parts socket mounted • Serviced from front.

CIRCLE 63 ON INQUIRY CARD

MATRIX



PROGRAM BOARDS

RAPID AND CONVENIENT PROGRAMMING/SWITCHING AT LOW COST

STANDARD .250" grid
MINIATURE .130" grid

Programming/Switching is performed by simply inserting Diode or Shorting Pins into contact matrix • Used as input-output switches and programmable diode matrices • Rugged and Reliable • 2 to 8 contact levels available • Matrices to 100 X 100.

CIRCLE 64 ON INQUIRY CARD

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"LINKS BETWEEN MAN AND MACHINE"

INFO-LITE CORPORATION

46-10 104th STREET • CORONA, N.Y. 11368

PRODUCTS

MULTIFUNCTION OPERATOR

Offering users the transfer function $E_{out} = Y_{in} (Z_{in}/X_{in})^M$ where M can range from 0.2 to 5 and is user-selectable through an external resistor network, MF435 features a wide dynamic range (up to 1000:1), accuracy of up to 2 mV ±0.1% of output, and frequency response of up to 20 kHz. An internal, precision 10 Vdc ±0.05% reference is provided for use as a constant at any of the inputs. Packaged in compact, epoxy-filled housings, modules can be mounted in mating sockets or soldered directly onto a PC board. **Intronics, Inc,** 57 Chapel St, Newton, MA 02158.
Circle 230 on Inquiry Card

DATA TRANSMISSION ERROR CONTROL UNIT

Model 9000 high speed error control units insure bit-error rates of $<10^{-12}$ for broadband transmission speeds up to 72 kilobits/s. Operating in half-duplex mode over 4-wire full-duplex lines, units use a low redundancy detection code with correction by ARQ to maintain throughput efficiency at 90% under normal operating conditions. A 1000-byte memory enables transmission continuity for loop delays up to 50 ms at 72 kilobits/s. Std units interface with Bell 303 broadband data stations. **American Computer Communications Co, Inc,** 2200 Lockbourne Rd, Columbus, OH 43207.
Circle 231 on Inquiry Card

LSI ASYNCHRONOUS TRANSCEIVER

The MP1013 universal transceiver, which handles asynchronous, full-duplex communications at up to 40 kilobaud, is a second source to General Instrument's AY-5-1013. Completely DTL/TTL compatible and requiring no interfacing circuits, the device accepts serial-bit char from a terminal or computer, and receives and transmits the char. Char comprise a start bit, five to eight data bits, one or two stop bits, and a parity bit. Baud rate, number of data bits, parity mode, and number of stop bits are programmed externally. **Plessey Semiconductors,** 1674 McGaw Ave, Santa Ana, CA 92705.
Circle 232 on Inquiry Card

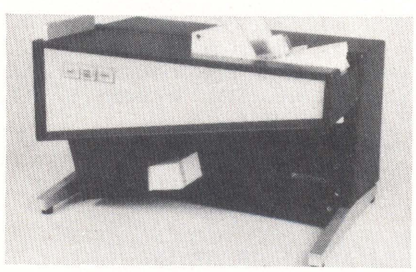
MULTI-LINGUAL VOICE SYSTEM

Votrax ML-I produces electronically synthesized speech with unlimited vocabulary. First foreign language available is German; plans call for development of Spanish, French, Italian, Japanese, and Farci. Designed to convert the output of a computer or other digital device into electronically synthesized human speech, it produces continuous speech output from a 300-bit/s data rate. Input is in the form of std ASCII char; inflection, speech rate, and volume are variable under software program control. **Vocal Interface Div of Federal Screw Works,** 500 Stephenson Hwy, Suite 102, Troy, MI 48084.
Circle 233 on Inquiry Card

FLATPACK PIN-DIODE SWITCH AND DRIVER

Featuring 50- to 400-MHz operation, the ISD 23702FSA contains an spdt switch and driver designed for rf control in the 50- to 400-MHz frequency range. The unit provides low loss and high isolation for applications on PC boards or stripline circuits as modules and in packaged switches. No bias connections or dc blocks are required in the rf line. Other features include TTL compatibility, <5-μs switch speed, 1.3 VSWR max. **LRC, Inc,** 1001 Digital Dr, Hudson, NH 03051.
Circle 234 on Inquiry Card

CARD READER FOR DATA ENTRY SYSTEM



A tabletop card reader that expands input capabilities of series 1300 data entry systems, the model 2510 reads 80-col punched cards at 300/min. Controls include power, reset, and halt switches. In addition, a card reader busy status light indicates hopper empty, stacker full, power off, card jam, and reader check conditions. The reader is transparent to series 1300 operating systems; installation involves only a single card adapter and cable interconnection. **Inforex, Inc,** 21 North Ave, Burlington, MA 01803.
Circle 235 on Inquiry Card

12-BIT D-A CONVERTERS

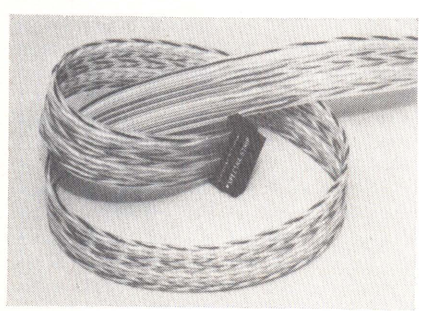
Featuring ±½ LSB linearity and ±0.3% absolute accuracy, worst-case over the full operating range, MN3200 devices are hermetically packaged in 18-pin DIPs measuring 0.5 x 1 x 0.175". Complete with internal reference supply and output op amp, the converters are functionally trimmed by laser as completed units to compensate all errors for range and zero offset and provide adjustment-free operation. Users need provide only the ±15-V power supplies. **Micro Networks Corp,** 324 Clark St, Worcester, MA 01606.
Circle 236 on Inquiry Card

APL/ASCII VIDEO TERMINAL

Designed for bit-paired applications, terminal includes true APL overstrike capability and underlining. Backspace through to previous line is std, and horizontal tabulation operates in 8-char increments. An APL/ASCII version of the Elite 1520A, the unit operates in conversational mode and displays 1920 char in 24-line x 80-char format. Other features include 128-char set, high resolution display, dual data rates to 9600 bits/s, and RS-232 interface. **Datamedia Corp,** 7300 N Crescent Blvd, Pennsauken, NJ 08110.
Circle 237 on Inquiry Card

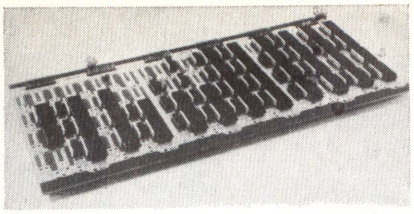
TWISTED-PAIR FLAT CABLE

Twist 'n' Flat™ combines twisted pairs of PVC-insulated conductors with lengths of parallel conductors in a laminated cable that can be used with instant-termination, insulation-displacement connectors (IDCs). It enables use of twisted-pair "3C"™ (controlled char cable) for greater control of signal-line crosstalk with IDCs, which terminate all conductors in the cable simultaneously, without stripping or other conductor preparation. **Spectra-Strip Corp,** 7100 Lampson Ave, Garden Grove, CA 92641.



Circle 238 on Inquiry Card

ECL/SIP PANELS FOR LARGE ARRAY MULTIPLICATION

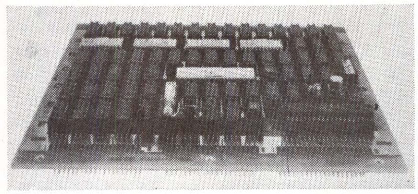


Twelve boards, designated 8136-ECL24 series, are available in patterns of 32, 64, or 96 in either 2- or 3-level wirewrap terminations. They accommodate up to 48, 24- and 16-pin devices, with positions for 8- and 12-pin single-inline package resistor networks for parallel termination to a −2-V power supply. Provision is included for mounting high frequency and electrolytic decoupling capacitors for a −5- or −2-V bus. All power busing is accomplished through expanded copper planes. **Augat Inc,** PO Box 779, 33 Perry Ave, Attleboro, MA 02703.
Circle 239 on Inquiry Card

VIDEO WORD PROCESSOR

In addition to insert, delete, word wraparound, move, search, roll-scroll, forms handling, and overlapped memory for simultaneous composing/hardcopy production, this processor provides mix and match of such peripherals as mag tape cartridge, mag tape cassette, IBM-compatible mag cards, floppy disc, paper tape, and more. Rather than breaking a word at the end of a line, the unit moves the entire word to the next line. It can delete an entire block of words, move a block (or char) to another location, search for errors (eg, keeping upper case consistent in every use), and compress or expand margins. **Tycom Systems Corp,** 26 Just Rd, Fairfield, NJ 07006.
Circle 240 on Inquiry Card

MICROCOMPUTER SYSTEM



Micromite is built on an 8 x 8½" wirewrapped socket panel that is said to minimize the need for interconnections and permit easy modification. The system accepts any 14- or 40-pin configuration and can be updated for higher density elements. It is available as a basic wirewrapped board, without components; or with an Intel 8080 microprocessor, 2K RAM, 1K p/ROM, 8-bit input port, 8-bit output port, UART channel, and RS-232 or TTY interface. **Data Numerics Inc,** 141-A Central Ave, Farmingdale, NY 11735.
Circle 241 on Inquiry Card

SLIDE ACTION DIP SWITCH

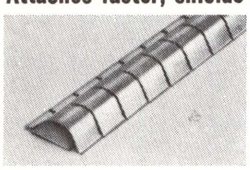
Series SL feature a depression in the slide button which insures tool self-centering and prevents slippage during actuation. Other features include flow-soldering and flux-washout capability provided by combination of UL-rated polyester case and standoffs and integral drain holes. Tease-resistant overcenter design switch action gives positive make or break, positive detect for tactile feel. Slide design prevents dust entry and reduces need for protective covering. **Control Switch, a Cutler-Hammer co,** 1420 Delmar Dr, Folcroft, PA 19032.
Circle 242 on Inquiry Card

PERMANENT MAGNET MOTOR

Series HCR has a 1/15-hp continuous-duty rating and a running speed of 3950 to 8160 rpm. Designed for dc operation, it is particularly adaptable to battery-power applications. Mechanical features include double-shielded and life-lubricated bearings, precision-ground stainless steel shafts, replaceable brushes, and a choice of tapped holes or flange mounting. Std designs are available with planetary and right-angle gear reductions. The motor can conform to commercial specs, UL, or applicable provisions of MIL-M-8609 or -E-5272. **Wertronix Corp,** 2673 Culver Ave, Dayton, OH 45429.
Circle 243 on Inquiry Card

When RFI problems get sticky, try sticky fingers®

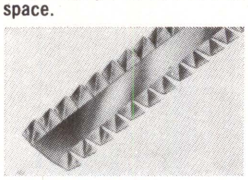
Attaches faster, shields better than anything else!



SERIES 97-500 The original Sticky Fingers with superior shielding effectiveness.

SERIES 97-520 A smaller size strip; highly effective in less space.

SERIES 97-555 New Single-Twist Series for use when space is at a premium. Measures a scant 3/8" wide.



SERIES 97-560 New ½" wide Double-Twist Series, ideal for panel divider bar cabinets.

Now you can specify the exact type beryllium copper gasket that solves just about every RFI/EMI problem. Perfect for quick, simple installation; ideal for retro-fitting. Self-adhesive eliminates need for special tools or fasteners. Write for free samples and catalog.

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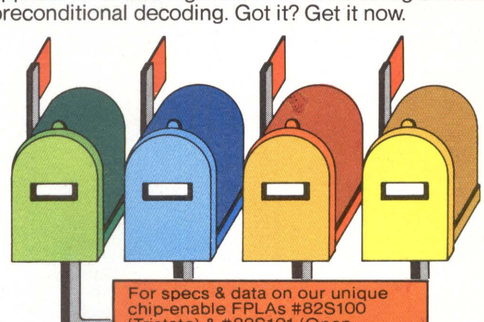
CIRCLE 65 ON INQUIRY CARD

MEMORY SERIES NO. 11

WHAT ARE 16 INPUT VARIABLES WORTH IN OUR FPLA'S?

Four times the address-scan capability of competitive Field Programmable Logic Arrays. As a bonus you get chip enable. Simplifies expansion of our 48 product terms and 16 input variables. Permits tristate application in bus organization. Provides logic inhibit, preconditional decoding. Got it? Get it now.



For specs & data on our unique chip-enable FPLAs #82S100 (Tristate) & #82S101 (Open Collector), attach coupon to letterhead.

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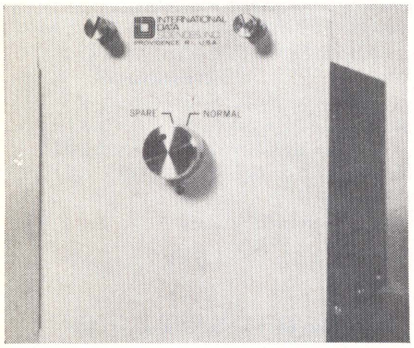
CIRCLE 66 ON INQUIRY CARD

SPARE MODEM BACKUP SWITCH

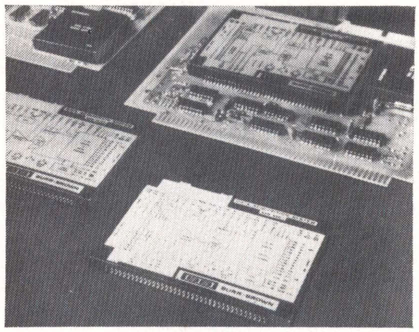


Model 8509 allows a single spare modem to be switched in to replace any one of a group of online modems by use of a front panel switch. The switch is compatible with all modules in the series 8500 EIA switch patch and monitor systems. Dimensions are 4 x 5¼ x 7½". Up to four modules may be mounted in a 8503-8 module cage and subsequently mounted in a 19" relay rack. The device simultaneously switches both EIA, RS-232 and telephone line interfaces. **International Data Sciences, Inc**, 100 Nashua St, Providence, RI 02904.

Circle 244 on Inquiry Card

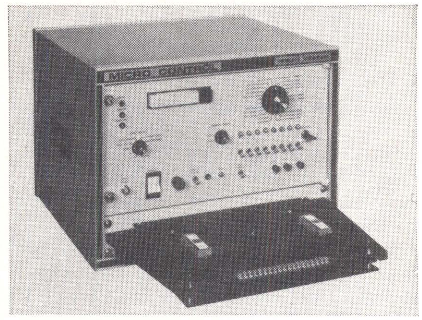
12-BIT DATA ACQUISITION UNITS WITH IC CONVERTERS

Two systems contain all components necessary to multiplex, sample, and convert ±10-V analog data from 16 single-ended (SDM850) or eight differential (SDM851) sources. Digital output is 12-bit parallel at throughput sampling rates of >50,000/s. Systems contain an analog multiplexer, differential amp, sample/hold, 12-bit A-D converter with reference, and programming logic. Either can be operated in continuous sequential sampling mode with no external components or controlled by a digital computer with random channel access. **Burr-Brown,** Box 11400, Tucson, AZ 85734.



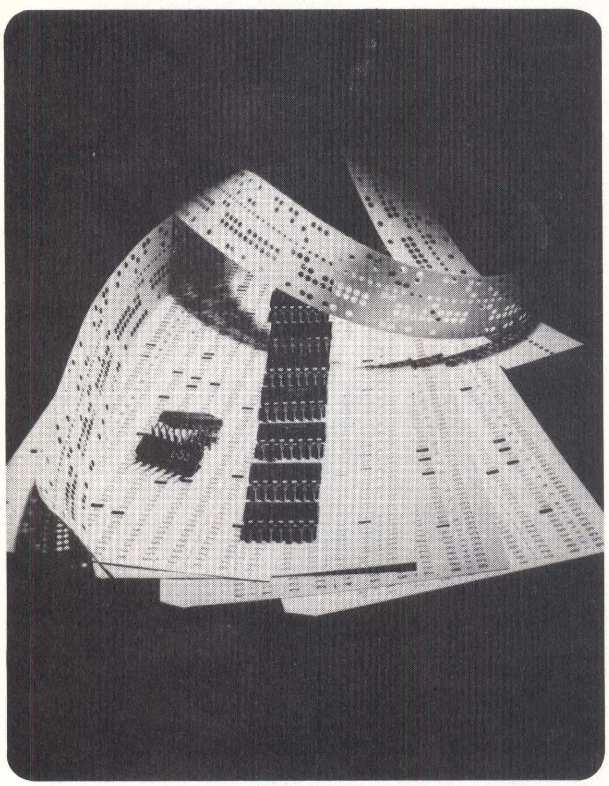
Circle 245 on Inquiry Card

BENCHTOP MICROPROCESSOR TESTER



MPU-1 tester and software development system compares the chip under test with a std microprocessor chip. Tests use worst-case voltages and timing, including fast and slow rep rates. Test programs are stored in 4K RAM, loaded from a TTY. The tester adapts to most microprocessor chips, and features complete panel controls for entering and displaying data, plus step mode for manually stepping through programs and facilities for debugging new programs including program breakpoint. **Micro Controls Co,** 1601 37th Ave NE, Minneapolis, MN 55421.

Circle 246 on Inquiry Card



"TTL-155"

Transistorized Logic Elements from the USSR

Error-Free Electronic Performance

- 100% quality control by every rating
- minimum power consumption
- minimum on-off time
- lightweight
- wide temperature range
- extra strong structure

Delay, ps:	
on	15
off	22
Max. voltage:	
supply	+5.5V
input	+4.5V
Max. output current, mA:	
high level	1
low level	16
Moise voltage, V:	0.4
Static power per one element:	25 mW
Dimensions, mm	19.5x6.5x3.8

Working temperature range, °C	−10 to +70
Acceleration, g:	
At vibration within frequency range:	
5 to 2000 Hz	10
at repeated impacts	35
at linear acceleration	50
at single impacts	150

"TTL-155" Integrated Microcircuits have been designed for computers and automatic controls—transistorized logic elements that meet the world's highest standards. Supplied in any quantities by: V/O Electronorgtechnica, 32/34 Smolenskaya Sennaya, Moscow 121200, USSR. Telex: 7586.

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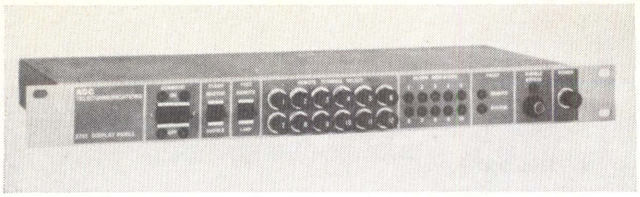
TELECOMMUNICATIONS ALARM/CONTROL SYSTEM



The 2711 alarm/control system automatically polls and controls up to 12 unmanned remote sites from a single master station. The device will warn of 120 alarm situations (up to 10 at each site) such as fire, equipment failure, or carrier dropout. The master terminal will control 24 separate remote functions (two per remote site). The complete system requires only a single voice-grade circuit (half-duplex FSK) to identify all alarms and provide remote control of command functions. Std features include programmable addressing of all remote sites from the master location, day/night submaster switching for unattended operation, and automatic scanning and fault identification. Master display and remote units each require one rack space; the master terminal takes three. **ADC Telecommunications, Alarm and Telemetry Systems,** 4900 W 78th St, Minneapolis, MN 55435.
Circle 247 on Inquiry Card

OPTICAL FIBER WAVEGUIDES

S20 series FIBERGUIDE is a multimode glass fiber available in continuous lengths from 100 to 1000 m, with transmission losses of <20 dB/km at a wavelength of 0.8 μ. Jacketed with EVA or PFA teflon, std waveguide can be used for optical transmission of information in either analog or digital form. Special optical waveguides are available with losses below 20 dB/km, as are fibers designed for high data rate transmission. Specs include 0.16 numerical aperture, 1.45 core index of refraction, 90-μ outside fiber dia and 44-μ core dia. Outside jacket dia is 0.4 mm (PFA) or 0.25 mm (EVA). Termination is cleaved flat. **Fiber Communications, Inc,** 391 Lakeside Ave, Orange, NJ 07050.
Circle 248 on Inquiry Card

MICROPROCESSOR-BASED TIMER/COUNTER

Using an Intel 4004 4-bit microprocessor chip to replace std TTL logic, series 9000 provides all std timer/counter features, reciprocating counter, and calculator in one package, and offers extended interfacing options and operating capabilities. Model 9015 is capable of measuring frequencies up to 100 MHz; the 9035 has a frequency range of up to 512 MHz. The instruments use a calculator-type keyboard located in a front-panel drawer for function control. An 11-digit, 0.43" yellow LED display provides numeric information while LED lamps are used as status indicators (to display function, measurement time, system control external references, input voltage range, slope, coupling, and separate/common indicators). Use of microprocessor allows the units to be interfaced via a g-p interface bus system, in parallel BCD format, in serial ASCII format for teleprinter; or in a do-it-yourself user option that provides extra high speed for custom requirements. **Dana Laboratories, Inc,** 2401 Campus Dr, Irvine, CA 92664.
Circle 249 on Inquiry Card

PACIFIC Electronics
AC POWER
Sources
Line Conditioners
Frequency Changers
Model 105-D
500 VA
Only $1495
500 VA
FEATURES:
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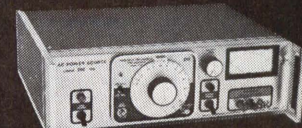
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CIRCLE 68 ON INQUIRY CARD

MEMORY SERIES No. 1
THE DO-IT-YOURSELF 2K PROM
Program it on your own home ground. With our big, fast, Field Programmable 512x4 PROM. #82S130/131. Twice the memory for your money: 2048 bits with same pins, same high performance rating as a 1K PROM.

Coupon clipped to letterhead gets you data sheet on #82S130/131—2K PROM.
Name
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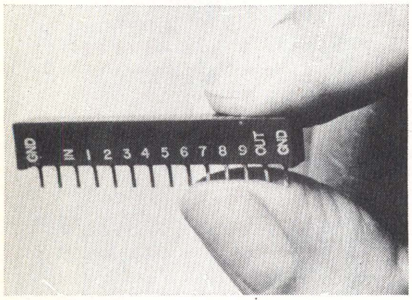
811 E. ARQUES, SUNNYVALE, CALIF. 94086

LUMPED CONSTANT DELAY LINE



Featuring single-inline design, SIL series are 10-tap epoxy-encapsulated modules that stand 0.25" off the board, measure 0.19 x 1.445", and meet environmental requirements of MIL-D-23859. Input impedances are 50, 100, or 200 Ω; total delay ranges from 20 to 200 ns with delay-to-risetime ratios of 4:1 min; delay time per tap ranges from 2 to 20 ns; max net risetime is from 4 to 37 ns; max dc resistance is between 1 and 9 Ω (depending on model); max distortions at any tap is ±15%; and attenuation varies from 2 to 10%. **Pulse Engineering Inc,** PO Box 12235, San Diego, CA 92112.
Circle 250 on Inquiry Card

TRANSCEIVER

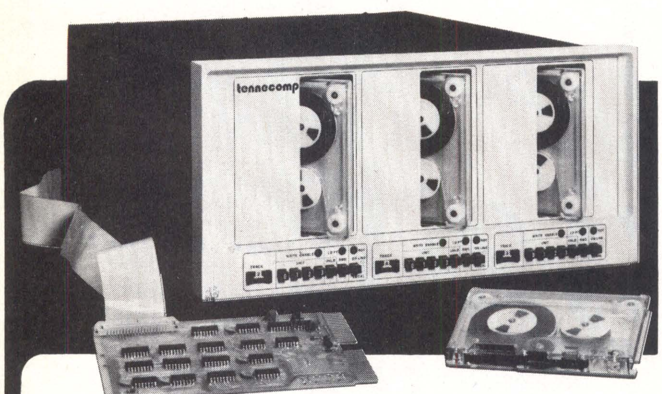
Series 500 provides high speed data communication via coax cable at data rates from 1.5 to 50 megabits/s. Six models facilitate digital transmission at 50 megabits/s to 500 ft. Multiple transceivers can be attached to a single coax data trunk. A conventional serial data interface allows attachment of a broad range of equipment. **Network Systems Corp,** 315 N Pierce St, St. Paul, MN 55104.
Circle 251 on Inquiry Card

HiNIL PULSE STRETCHER

The 349 high noise immunity logic bipolar IC can be used to stretch either positive or negative input pulses to those of longer duration. It delivers timed output pulses whose widths are equal to the sum of the input pulse width and a fixed pulse stretching time determined by an external resistor and capacitor. Stretching range is 100 ns to 0.5 s; however, the length of the output pulse can be extended indefinitely by retriggering the device before it times out. **Teledyne Semiconductor,** 1300 Terra Bella Ave, Mountain View, CA 94303.
Circle 252 on Inquiry Card

COMPUTER-CONTROLLED BAR CODE PRINTER

A computer-keyboard input printer of bar codes for optical scanning, including additional lines of alphanumeric legend, the unit uses carrier-supported ink (CSI™) to guarantee black smearproof marks on vinyl, coated paper. Kromekote, self-destructibles, and similar pressure-sensitive label stocks as well as tag stock. Die-cut labels can be >4" high. The printer can print three lines of alphanumeric legend plus a bar code and its related digits; and provides capability for random printing of Arabic digits up to ¾" high. **Scanmark/Markem Corp,** 150 Congress St, Keene, NH 03431.
Circle 253 on Inquiry Card



the new DataPacer™ magnetic tape system sets the pace on the bottom line.

for system buyers:

Big 3M data cartridge capacity of 2.8 million bytes.

High speed read or write of 30 ips with transfer rate of 48,000 bps. Search at 90 ips.

Precise stop-and-go bidirectional operation cuts access time in search and retrieval.

Operational control comparable to half-inch drives with unit selection, on-line/local selection and off-line rewind.

Complete DEC-compatible software package.

Performance far surpasses cassette standards, at a cassette price: from $2980.

or system builders:

Small, compact and modular, up to three data cartridges across a 19-inch rack.

Single cable, single card plug-in interfacing for PDP-8 or PDP-11 minicomputers.

Automatic CRC error detection, dual gap read-after-write recording head, phase encoding. Meets proposed ANSI standards.

Simple, reliable transport, field-proven on thousands of units.

Fast, easy installation and maintenance.

Performance far surpasses cassette standards, at a cassette price: from $2980.

Write or call for complete information.

TENNECOMP SYSTEMS INC.

795 Oak Ridge Turnpike Oak Ridge, Tennessee 37830
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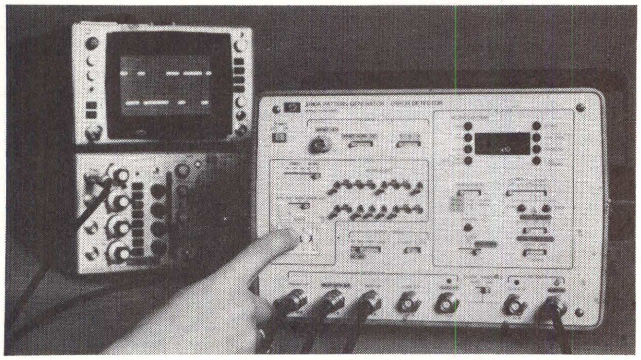
PORTABLE PCM/TDM TRANSMISSION TEST SET



Model 3780A pattern generator/error detector measures binary errors and code violation errors in digital transmission and terminal equipment operating at bit rates between 1 kilobyte/s and 50 megabyte/s. Frequency offset generation and measurement is also available at std bit rates used in PCM/TDM transmission. Both ternary coded (HDB3, B6ZS, AMI) and binary interfaces are provided. Bit error rate or total error count can be displayed directly or monitored via a BCD printer and stripchart recorder, allowing unattended long-term measurements of error distribution. The device provides three internal crystal clocks and clock recovery at std bit rates in the 1.5- to 50-megabit/s range. Error measurements can be made with PRBS or WORD patterns; the receiver has automatic pattern recognition and synchronization. **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.

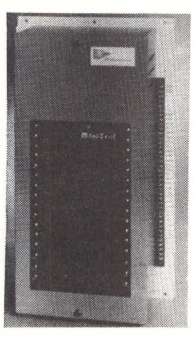
Circle 254 on Inquiry Card

SWITCHING POWER SUPPLIES

MG power supplies are available in ratings of 5 to 24 Vdc at 10, 20, 40, and 60 A; the triple-output MGT is available at 5-Vdc, 20-A main output and either ±12- or ±15-Vdc auxiliary outputs. Small sizes are achieved in the MG series by rectifying the input voltage directly and replacing the series element by a pulse width modulated inverter circuit. Isolation is maintained by the use of a screened transformer in the inverter stage and efficiency is further improved by use of high performance diodes as the final rectifying elements. MGT supplies deliver 5 V at 20 A using pure switching techniques and two 15-V outputs at 1.75 A via linear regulators. **Gould Inc, Allied Control Div,** 100 Relay Rd, Plantsville, CT 06479.

Circle 255 on Inquiry Card

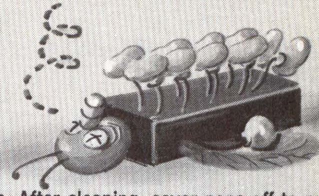
LOW COST PROGRAMMABLE CONTROLLER



MiniTrol, a completely packaged, small programmable controller with I/O flexibility, is designed to provide economical automatic digital control. Basic unit consists of power supply, 256 words of p/ROM and eight inputs and eight outputs in a single enclosure. Design features include plug-in expandable I/O, in increments of one, up to 128 and in any mix; plug-in expandable memory, in increments of 256 words, up to 1024; plug-in interchangeable CMOS read/write memory and p/ROM and built-in continuous automatic self-test. One program loader accommodates both read/write and read-only memories. **I•T•E Datametrics,** 340 Fordham Rd, Wilmington, MA 01887.

Circle 256 on Inquiry Card

we got the bugs out of D.I.P. switches



Most common bug in dual in-line program (D.I.P.) switches is open circuits caused by solder, flux, solvent, etc. contamination penetrating the switch during installation. Licon sealing solved the problem. Ultrasonically welded base and cover junctions and molded-in terminals. 9 Licon® Standard D.I.P. Switch models available with "pop-top" cover for top and bottom protection. After cleaning, cover pops off to program switch. Low profile . . . only .280 inches high. 2 through 10 pole range. Slide detent mechanism provides positive feel actuation for open and closed position. Detents lock to prevent accidental actuation. Quick open/closed visual indication. .100 x .300 inch terminal spacing for easy board insertion. Save space. Snap-on dust covers available for after-installation use. 4 unique L.E.D. LPB models available for press-to-test applications. Call local Licon rep or distributor or write for details. Licon, A Division of Illinois Tool Works Inc., 6615 W. Irving Park Road, Chicago, Illinois 60634. Phone: (312) 282-4040. TWX 910-221-0275.

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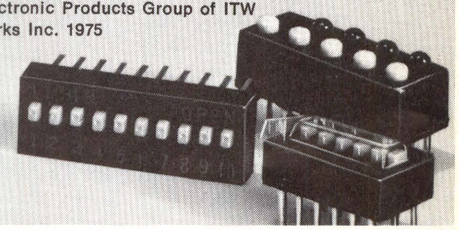

CIRCLE 72 ON INQUIRY CARD

MEMORY SERIES No. 10

GIANT 4K PROMS EVEN PRODUCTION CAN AFFORD.

Take the large economy size to prototype OR production. 4096 bits at 60ns secures patterns faster; 512 x 8 organization shrinks board space, boosts reliability—saves parts/assembly costs, speeds the line. #82S115, in volume stock.

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CIRCLE 73 ON INQUIRY CARD

SEMICONDUCTOR MEMORY FOR DEC COMPUTERS

High speed plug-compatible semiconductor memory systems for PDP-9 and -15 computers feature a 450-ns cycle time. 128K and interface requires only 10½" of panel space. Memory is supplied in 4K x 18-bit increments with 32K x 18-bits on each plug-in board. Memory chips as well as logic ICs are mounted in plug-in sockets for field replacement. Because the system uses static memory, power failure data retention circuitry can be a low power-consumption, battery power supply. **Dimensional Systems, Inc, Memory Div,** 6 Nevada Dr, Lake Success, NY 11040.
Circle 257 on Inquiry Card

MINICOMPUTER CORE MEMORIES

65-kilobyte add-in card memories for Interdata 74, 7/16, 7/32, and 8/32, Data General's Nova 2, 800, and 1200 series, and Digital Computer Controls' D-116 series minicomputers feature 240-ns access and 650-ns cycle times. Package size is <75 in.^{3}, and the memories are designed to be stacked at ½" centers. Cost-effectiveness has been achieved through reduction in number of slots occupied by the cards in a chassis, so that the user can use more peripherals, controllers, and other devices without having to overflow into another expansion chassis. **Pushpa International Corp,** 14142 Ipswich St, Westminster, CA 92683.
Circle 258 on Inquiry Card

4K p/ROMs

Organized as 512 words x 8 bits, and utilizing the company's avalanche-induced migration (AIM) technology for programming, IM5605 has open collector outputs, and the IM5625 is 3-state. Typ read cycle time for both is 45 ns at 25°C. Input and output dc characteristics are std TTL. Conventional bipolar TTL processing is employed, with no additional steps required to form AIM elements. Both devices are available over the 0 to 75°C temp range in ceramic DIL packages. **Intersil, Inc,** 10900 N Tantau Ave, Cupertino, CA 95014.
Circle 259 on Inquiry Card

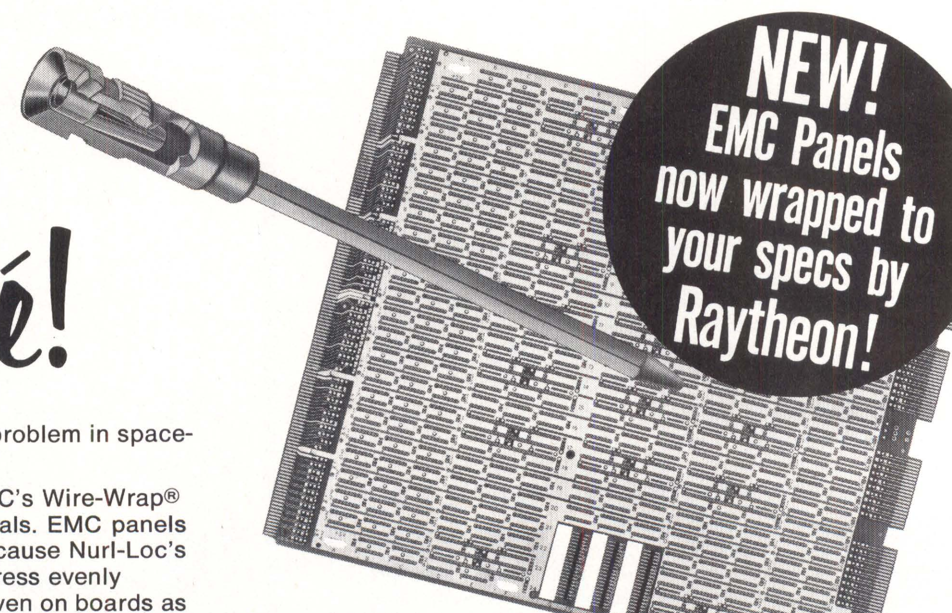
MULTIPLY/DIVIDE MODULE

The 8005 operates at either 2.3 or 5 μs. Multiplication and division are performed from specified memory registers. The module multiplies two 8-bit words, giving a 16-bit result, and divides a 16-bit word by an 8-bit word, giving a 16-bit result with an 8-bit remainder. An ALU and shift register combination implements multiplication and division. All logic, timing, and clocks are contained on the module. Operating speed prevents a std 8080 CPU from responding before the result is ready. **Gnat Computers,** 8869 Balboa Ave, Suite C, San Diego, CA 92123.
Circle 260 on Inquiry Card

LOW VOLTAGE SWITCHING POWER SUPPLIES

DLR (direct line rectification) series of modular dc switching power supplies features up to 85% operating efficiency. Models include 4.2 to 6, 6 to 11, 16 to 23, and 22 to 30 Vdc (500, 600, and 750 W). Input voltage is 115/230 Vac, 1ϕ, 47 to 1000 Hz; output ripple/noise is 2% pk-pk 0.5% rms max; transient response time is 0.5 ms; protection includes current limit and overvoltage; and full rated temp range is −20 to 40°C. Available optionally are 3ϕ operation, 300-Vdc input, 150-Vdc input for UPS-supported systems, thermal cutoff, and mil specs. **Electro-Module, Inc,** 2855 Metropolitan Pl, Pomona, CA 91767.
Circle 261 on Inquiry Card

Touché!



Target: to eliminate the warp problem in space-saving 1/16" plug-in panels.

The winning combination: EMC's Wire-Wrap® Panels with Nurl-Loc® Terminals. EMC panels stay flat, without stiffeners, because Nurl-Loc's splined cylinder distributes stress evenly throughout board thickness, even on boards as large as 15" x 18" (shown). A flat panel means more accurate true positioning between pins for better wrapping. Nurl-Loc also permits easy pin removal without damage. And the four-finger contact holds any I.C. lead firmly, even as small as .011 dia. Call Allan Klepper (401) 769-3800 for your copy of the interesting and informative "Inside Story", or write Electronic Molding Corp., 96 Mill St., Woonsocket, Rhode Island 02895.

EMC's Wire-Wrap® Panels with Nurl-Loc® Terminals ... better performance by design!

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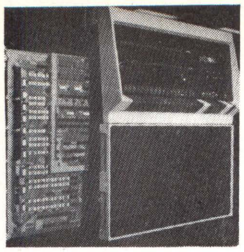
CIRCLE 74 ON INQUIRY CARD

WRITABLE CONTROL STORE



A 2-board add-on option for PDP-11/40 computers, the WCS 11/40 plugs into the processor and provides 1024 words of 80-bit read/write microprogram memory, implemented with 50-ns TTL RAM. All processor data paths are available to user microprograms running in the option. Additional data paths implemented in the unit include 16-bit shift/mask for field isolation, N-way branching on data fields, a literal field, and a 16-level micro stack. The option can be used for extending or modifying the -11/40's instruction set, or for emulating other machines. The unit has a 160- to 320-ns microcycle time. Included with the option are software and documentation for developing and debugging user microprograms, as well as maintenance documents and diagnostic programs. **Three Rivers Computer Corp,** Box 235, Schenley Pk, Pittsburgh, PA 15213.

Circle 262 on Inquiry Card

DIGITIZER KEYBOARD CURSOR

To facilitate entry of numerical data while digitizing maps and charts, a keyboard has been incorporated in a cursor for use with the Gradicon free cursor digitizer. The cursor is used to locate and follow scribe marks on the mylar film; the digitizer senses cursor position and converts coordinate data into digital form for computer processing; and the keyboard permits numerical data to be entered concurrently with coordinate data. The keyboard includes 10 numerical keys, decimal point and minus sign keys, four function keys, a clear key, and a 10-digit readout display. In use, the operator enters values on the keyboard, centers the scribe point over the position, and presses the scribe arm down, entering X-Y positional coordinates plus its associated value into the data stream. **Instronics Inc,** 1 Regency Dr, Bloomfield, CT 06002.

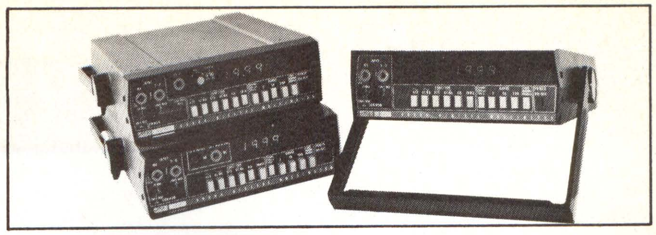
Circle 263 on Inquiry Card

THREE-PROCESSOR COMPUTER FOR SEVERE ENVIRONMENTS

Heart of the 1664 (AN/UYK-28) is a hardware-variable, precision floating-point processor, which operates simultaneously with a microprogrammed g-p processor and a direct memory access processor. Features include executive mode for complete memory access and I/O protection, significantly expanded instruction set, extensive I/O capabilities, and complete software support. Total memory addressability is 512 kilobytes. Main memory is available in 16K increments; up to 128K can be directly addressed. Operating systems and languages include SOS (stand-alone operating system) which contains I/O drivers or peripherals; RTOS, a small memory-resident g-p multitask monitor for real-time environments; and RDOS which supports all major peripherals, programs, and languages. **Rolm Corp,** 18922 Forge Dr, Cupertino, CA 95014.

Circle 264 on Inquiry Card

Fluke Model 8000A



No other DMM offers you all of these outstanding specs in one box

- Best accuracy statement of any 3½ digit DMM: 0.1% accuracy ± 1 digit; one year accuracy time span; 25° C ± 10° C accuracy temperature span.
- Normal mode rejection: 60 dB at 50 and 60 Hz.
- Common mode rejection: 120 dB with 1 KΩ unbalance.
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- 26 ranges of volts, amps and ohms.
- More option power than any other DMM. Includes low ohms option with 1 milliohm resolution. 20 amp ac/dc current capability. BCD output. Built-in rechargeable battery pack.
- More accessories than any other DMM. Includes 600 amp AC clamp-on current probe. 40 KV high voltage probe. 100 and 500 MHz rf probes.
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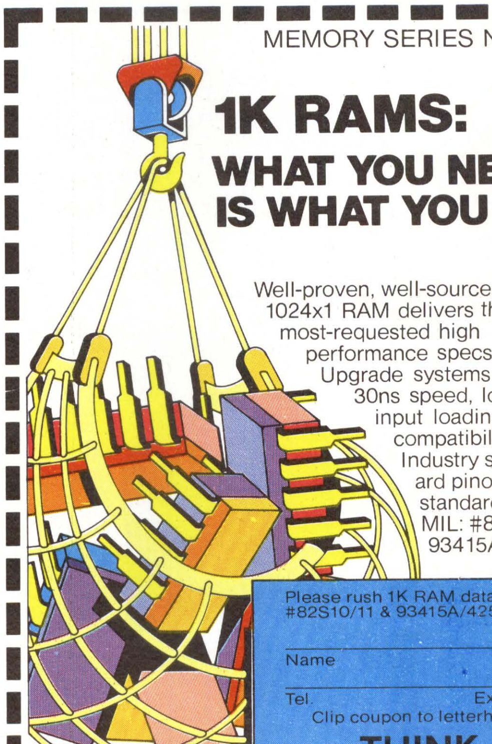
For literature only, Circle 94 on Inquiry Card.

MEMORY SERIES No. 2



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Well-proven, well-sourced, this 1024x1 RAM delivers the most-requested high performance specs. Upgrade systems with 30ns speed, low input loading, TTL compatibility. Industry standard pinouts, standards or MIL: #82S10/11; 93415A/425A.

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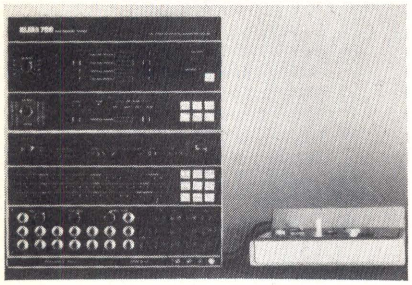
PRODUCTS

LOW COST MEMORY TESTER



Diagnostic and high volume parametric/ functional test capabilities are combined in the 760 modular memory test system. Limit boards and adapters are utilized to test MOS, TTL, and ECL RAMs. Test capability is extended to shift registers via microprogram boards, and to ROMs with a "self-learning" subsystem. A test deck interfaces with autohandlers and wafer probers, and a variety of optional diagnostic modules is available. A 48-bit wide x 64-address deep microprogrammer produces barber pole, checkerboard, walking columns, and other complex patterns. **Alma, div of Develco, Inc,** 530 Logue Ave, Mountain View, CA 94043.

Circle 265 on Inquiry Card

130/260-BIT CHARGE-COUPLED ANALOG SHIFT REGISTER

Designed to eliminate the need to convert analog signals to digital form for delay within a digital delay system and then to reconvert to analog form, CCD311 performs the function of a wide-range variable analog delay line. Delay is determined solely by the frequency of an external clock signal. The circuit utilizes buried-channel, charge-coupled technology. Operation ranges from 10-kHz frequencies to 15-MHz video rates. Delay time range of from 20 μs to 25 ms can be obtained by varying the clock rate. **Fairchild Camera & Instrument Corp, Integrated Circuits Group,** 464 Ellis St, Mountain View, CA 94042.

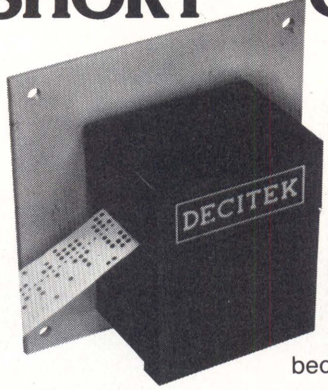
Circle 266 on Inquiry Card

REAL-TIME COMPUTER

The SLASH 7's asynchronous CPU has instruction prefetch and interleaved core memory to provide an effective cycle time of 425 ns. CPU options include multiported memory in both core and semiconductor. Semiconductor memory may transfer at 4.8 megabytes/s on one port, or interleaved multiple channels at 15 megabytes/s. Software includes resident, tape, disc, and disc monitor (DMS) operating systems. **Harris Corp, Computer Systems Div,** 1200 Gateway Dr, Fort Lauderdale, FL 33309.

Circle 267 on Inquiry Card

SAM IS THE LOWEST PRICED READER YOU CAN BUY. BUT YOU DON'T GET SHORT CHANGED.



You could spend a lot more for a tape reader and still not get all of SAM'S quality features. SAM clips along at 300 cps, has our sure-footed dual sprocket drive and our state-of-the-art fiber optic light source and photo transistor read head. We can make SAM do all this *and* save you money because we do things differently.

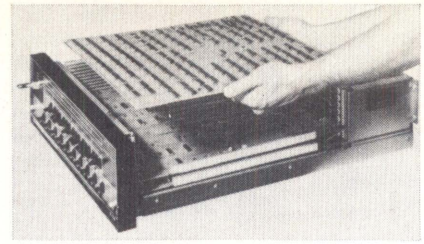
This is the plain, brown wrapper SAM comes in.

The more you know about punched tape equipment, the better you read us.

DECITEK

250 CHANDLER STREET, WORCESTER, MASSACHUSETTS 01602, U.S.A. (617) 798-8731

SINGLE-BOARD DISC CONTROLLER



The DC-220 universal disc controller is software compatible with Data General Nova and Eclipse computers plus DCC-116, Keronix, and other Data General-emulating computers. Plugged into a single slot inside the computer, it controls up to four single-platter cartridge drives, two dual-platter drives, or two single-platter or a single dual-platter drive each having 406 tracks/surface. Automatic seeking of the desired track is performed by simply issuing a DOA command. **Western Peripherals, Inc,** 2893 E La Palma Ave, Anaheim, CA 92806.

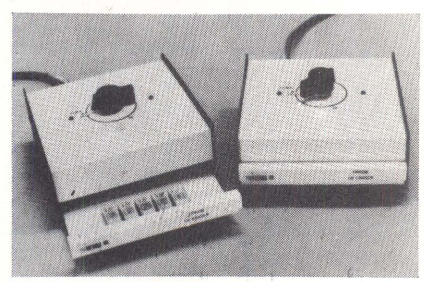
Circle 268 on Inquiry Card

OPTO-COUPLERS/ISOLATORS

Electronically and mechanically interchangeable with Monsanto MCT-2, STOC series offer 5-kV min isolation voltage. Packaged in a 0.3 x 0.35 x 0.125" plastic DIL case, each unit contains a GaAs LED that is optically coupled to a silicon npn phototransistor detector. Current transfer ratios range from 150% (100% min) to 30% (10% min). Rise times range from 8 to 2 to 20 μs, and collector-emitter saturation voltages are 0.4 and 0.6 V. **Sensor Technology, Inc,** 21012 Lassen St, Chatsworth, CA 91311.

Circle 269 on Inquiry Card

UV-ERASABLE p/ROM ERASER



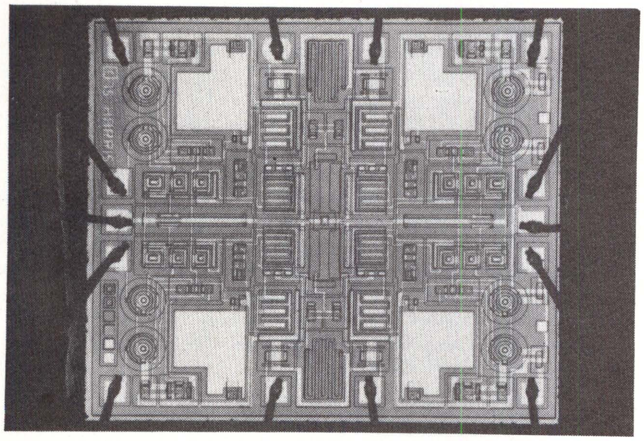
Capable of erasing devices rated at 6 W-s/cm^2 integrated erasure dose in <5 min., devices rated at 10 W-s/cm^2 in <10 min., with complete safety to devices and personnel, the device prevents damage using an adjustable timer which shuts off the UV source when the set-in time has elapsed. Safety to personnel is assured by a housing which prevents UV leakage and an interlock which shuts off the UV when the p/ROM drawer is opened. **Prometrics, Inc,** 5345 N Kedzie Ave, Chicago, IL 60625.

Circle 270 on Inquiry Card

DATA ACQUISITION SYSTEM

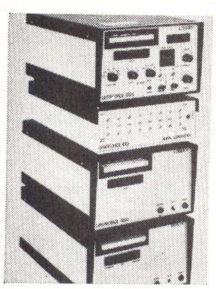
The 8-channel DAS400 provides 0.03% accuracy and 30-kHz/channel speed, as well as all necessary functions for data acquisition. Costs are kept down by omitting such features as sequential address counter and expandability; also eliminated are analog problems, including ground loop. Main components consist of A-D converter, sample/hold, and multiplexer; all are socket mounted and tested individually before assembly. Key specs include eight single-ended analog inputs, input voltage of 0 to 10 V, −5 to 5 V selected by logic level at polarity pin; 100-MΩ min input impedance, and 12-bit resolution. Tempcos are 15 ppm/°C linearity, and 30 ppm/°C gain. Max throughput rate is 30,000 channels/s with crosstalk of <½ LSB with 10 V pk-pk at 1 kHz. **Hybrid Systems Corp,** 22 Third Ave, Burlington, MA 01803.
Circle 271 on Inquiry Card

QUAD OPERATIONAL AMPLIFIER



With performance characteristics claimed to equal or exceed those of the std 741, the HA4741 combines 3.5-MHz bandwidth and 1.6-V/μs slew rate with low input voltage noise (9 nV/$\sqrt{Hz}$ typ) to provide a device suitable for both active filter and audio amp applications. Operational voltage range is ±2 to 20 V. Supply current maximums are 5 mA for military versions and 7 mA for commercial units. True differential inputs, and crossover distortion that is not detectable even at 50 kHz are features. Typ offset voltage of 0.5 mV and offset current of 15 nA enhance its operation in instrumentation equipment. The device comes in a 14-lead CERDIP and is pin-for-pin compatible with LM124, LM148, and MC 3403 series devices. **Harris Semiconductor, a div of Harris Corp,** PO Box 883, Melbourne, FL 32901.
Circle 272 on Inquiry Card

CASSETTE DATA HANDLING EQUIPMENT



Second-generation Dataforce recorders digitally record combinations of event, digital, and analog data, for replay at high speed to programmable calculator or minicomputer. Std and customized software is available to process data tapes recorded from common instrumentation. Designs provide flexible interfacing capability, improved selection of front panel controls, and convenient internal and rear panel access to logic control functions. The 008 event/analog input data recorder, which accepts and records one event and up to eight analog inputs in the ±1-V range, provides an 8-channel multiplexer, digital counter, scanner, A-D converter, front panel digital display, and digital cassette recorder in one enclosure. The unit has 20 crystal-controlled sampling rates between 100 ms and 26.6 min. **Nomal Data Systems Inc,** 1101A Air Way, Glendale, CA 91201.
Circle 273 on Inquiry Card

THE BEST IS NOW #1*

MFE's 250B Digital Tape Transport Offers a 32000BPS Data Transfer Rate

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□ 15,000 Hr. MTBF □ 1 Year warranty □ Two moving parts □ Reel to reel □ Constant tape tension and constant tape speed — servo controlled □ ±5VDC operation □ Guaranteed cassette interchangeability □ Up to 800 BPI □ Read after write heads □ Bi-directional read/write operation □ Size: 4.39" X 5.46" X 2.42" □ A few $525, a hundred $325 □ Call or write Jim Saret

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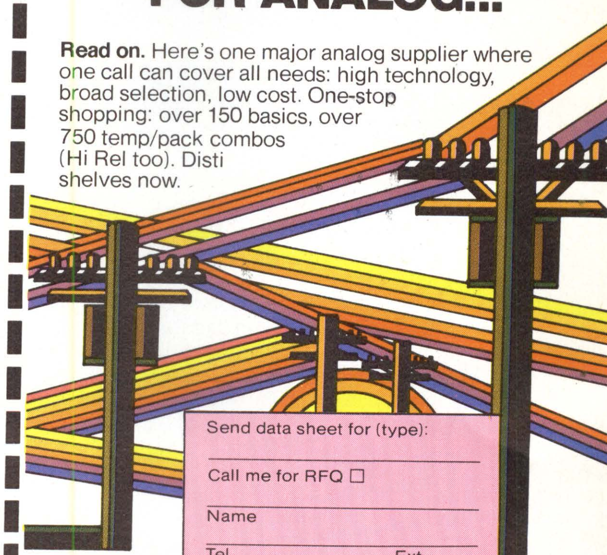

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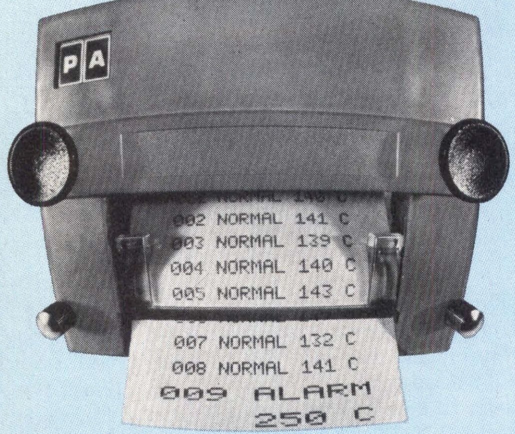
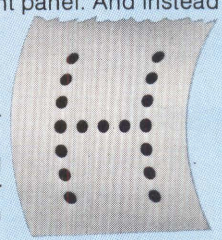


deserves another.

You flipped over our Matri-Dot alphanumeric mini for "first line down" data printing; now we've flipped our design to give you "first line up" text print format, too. So you're ahead, whatever your point of view. Because no one else makes printers as small as 3"H x 3½"W x 7"D. No one else sells them as low as $140 (in quantities of 100). And no one else offers our features. Instead of a drum, our unique print head purrs along at 138 lines per minute for 18 data columns, even faster for fewer columns. Instead of messy ribbons, our exclusive drop-in ink platen lasts for 75,000 lines and replaces from the front panel. And instead of engraved drum limitations, our 7 x 5 dot matrix characters provide full alphanumerics with a complete ASCII 63 character set. Enhanced characters are also available...8, 10, 12, or 14 characters per inch. All this, plus multiple-copying capabilities and plug-in panel mounting. No matter how you look at Matri-Dot, it's a turn for the better.



PA PRACTICAL AUTOMATION, INC.

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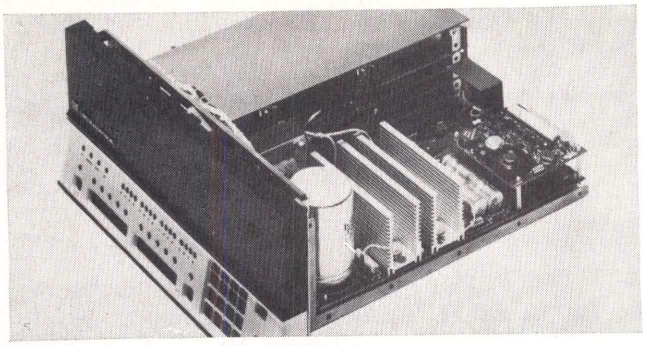
Tel: (203) 929-5381

PRODUCTS

SMALL MINICOMPUTERS

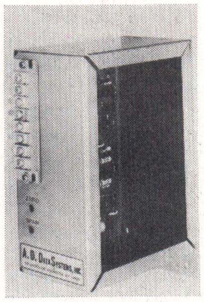


Alpha LSI-3/05 computers are packaged versions of the half-card Naked Milli. Designed with std TTL components, the devices come in three different series, each mounted in a chassis and featuring various memory sizes and types. The A series includes a half-card CPU, 10-A power supply, 3-slot motherboard, operator's console, and min of 256 16-bit words of MOS RAM on a half card with sockets for up to 8K of ROM chips; B series units have the same configuration but include a 15-A power supply, and a 5-slot chassis. C series models use the 5-slot chassis and 15-A power supply, and include a programmer's console instead of an operator's console. Various other configurations, including some with std full-size chassis, accommodate up to 32K 16-bit words of directly addressable memory. **Computer Automation, Inc**, 18651 Von Karman, Irvine, CA 92664.
Circle 274 on Inquiry Card

CONTAMINATION-PROOF PUSHBUTTON SWITCH

A PCB-mount pushbutton switch designed to withstand wave soldering and related cleaning processes, series 39-251 resists entry of contaminants because terminals are ultrasonically welded into the switch body. Top and bottom halves are molded in high temp polyester and are ultrasonically welded together. To complete the seal, an optional semi-rigid boot fits over the plunger. Occupying less than ½" sq, the momentary action switch has terminals located on 0.1" centers. The unit has N.O. and N.C. sections which can provide spdt, spst N.O., or spst N.C. contact circuitry. The gold-plated contact system makes and breaks a range of voltages and currents from logic level loads up to ¼ A for a min of 250,000 operations. **Grayhill, Inc**, 561 Hillgrove Ave, La Grange, IL 60525.
Circle 275 on Inquiry Card

ISOLATION TRANSMITTERS



Series 26 is available with all std process instrumentation I/O, plus a digital output in ASCII serial with 20-mA neutral line current, which allows any remote instrument to be connected by 2-wire lines over long distances to a central station without any signal error, and to be read directly on a teleprinter. Zero and gain adjustments are made through trimpots accessible through the front panel. Specs include 120-dB at 60-Hz common mode rejection; accuracy of 0.1% of span; and response time of <20 ms to 0.1% accuracy. Linearity is 0.1% of span; stability is 0.02%/°C. Input overload can be 200 Vdc or 110 Vac with no damage to circuits. Input to output isolation is rated at 1200 Vdc. **A. D. Data Systems, Inc**, 830 Linden Ave, Rochester, NY 14625.
Circle 276 on Inquiry Card

← CIRCLE 80 ON INQUIRY CARD

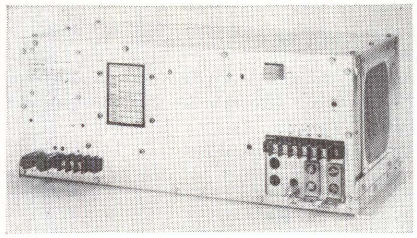
IC-PLUGGABLE ECL BOARDS

Pluggable packaging assemblies for high speed ECL I, II, and 10,000 logic series use a 3-layer low impedance power distribution system. Commercial design has a laminated third voltage plane; military design is of true multilayer construction, meeting MIL-P-55640. Signal interconnections are completed by std wirewrapping. **Garry Manufacturing Co,** 1010 Jersey Ave, New Brunswick, NJ 08902.
Circle 277 on Inquiry Card

ACTIVE POWER LINE FILTER

Overcoming problems of incoming spikes, voltage transients, and noise on ac-input power lines, filter tracks line voltage and switches into operation when an input transient exceeds a predetermined set voltage, which can be as low as 10 V pk. Operating over a wide temp range, with low 60-Hz leakage and no ground loops, the device accommodates std power line input voltages from 115 through 440 V rms, either single- or 3-phase. **Control Concepts Corp,** 333 Front St, Binghamton, NY 13905.
Circle 278 on Inquiry Card

DC POWER SUPPLY WITH BROWNOUT PROTECTION



HPB series Limitran™, which automatically regulates ac line voltage changes, uses a double regulator design to improve effectiveness and provide brownout protection. As the ac line voltage changes, the ac regulator switches transformer taps to meet the new line conditions. Zero voltage switching eliminates noise and voltage spikes, while a clock-through technique provides fast, stable operation. Voltage corrections are accomplished in half-cycle time periods. Specs include 85- to 125-V input range, >50% efficiency, 5- to 28-Vdc outputs at 50 to 18 A with 0.02% line/load regulation and 0.01% rms ripple. **Modular Power, Inc,** 4818 Ronson Ct, San Diego, CA 92111.
Circle 279 on Inquiry Card

DIGITAL LOGIC POWER SUPPLY

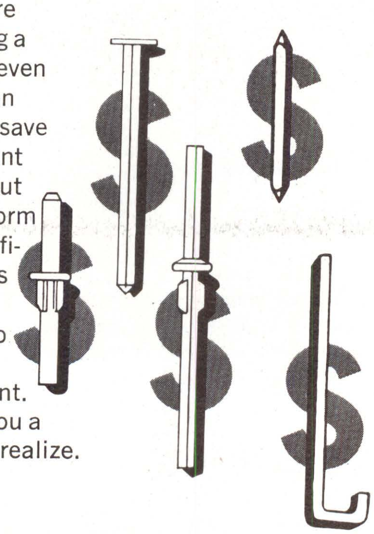
MPS-2A is designed to mount directly in a std card file with a 44-pin edge connector. Output voltage is 4.4 to 5.85 Vdc, overvoltage cutoff is 6.6 Vdc max in 11 μs max, output current is 2.5 A max, line regulation is ± 2 μV with 10% input change, load regulation is ± 2 μV no load to max load, timing reference signal is 12.5 V rect sine, and op temp range is 0 to 70°C. **Wyle Computer Products,** 3200 Magruder Blvd, Hampton, VA 23666.
Circle 280 on Inquiry Card

BAR CODE PRINTER

The 2150 bar code printer/applicator first prints on pressure-sensitive labels and then automatically applies them to products or packages, online. The system prints universal product code, Codabar, Plessey, two-out-of-five (several variations), and customer-specified codes. Input information can be transmitted from keyboard or remote computer, and can vary or be repeated as desired. **Compac Corp, Label-Aire Div,** 1016 S Vail Ave, Montebello, CA 90640.
Circle 281 on Inquiry Card

Why pay more for square wire terminals just because they're made on screw machines?

Screw machined parts are expensive. If you're using a square wire terminal (or even round wire parts) made on screw machines, we can save you money. Our equipment can upset, head, point, cut radii, knurl, flatten and form square wire to your specifications . . . and at far less cost. If you require, we'll supply the parts plated to suit your specifications. Send us a sample or a print. We may be able to save you a lot more money than you realize.



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CIRCLE 81 ON INQUIRY CARD

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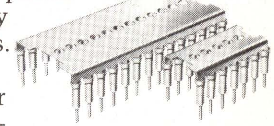

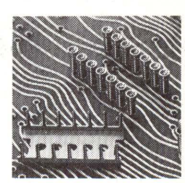

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CIRCLE 82 ON INQUIRY CARD

LITERATURE

Display Terminals

Catalog describing CRT display and terminal equipment details RO and KSR models available in six std display sizes, and outlines characteristics in chart form. **Ann Arbor Terminals, Inc**, Ann Arbor, Mich.
Circle 300 on Inquiry Card

SNA/SDLC

Introduction to Systems Network Architecture and Synchronous Data Link Control, for the telecommunications user in terms of how they will impact his network, is presented in booklet. **Sanders Associates, Inc, Data Systems Group**, Nashua, NH.
Circle 301 on Inquiry Card

Electronic Assembly Services

Illustrated brochure on wire harness and cable assembly facilities and circuit board production facilities also covers inspection and QC procedures as well as "clean room" packaging and mechanical assembly services. **Laminaire Corp**, Rahway, NJ.
Circle 302 on Inquiry Card

Phase-Locked Loop ICs

Booklet introduces PLL, describes a monolithic PLL device, and explains typ applications in frequency-shift, phase-shift, and tone-burst keying; frequency and amplitude modulation; and pulse-amplitude and pulsewidth modulation, suppressed carrier am, and delta modulation. **Plessey Semiconductors**, Santa Ana, Calif.
Circle 303 on Inquiry Card

Acoustic Telephone Coupler

Detailing acoustic coupling at 1200 baud, brochure outlines such features as automatic line turnaround and reverse channel, and shows how advanced filtering and transmitter design eliminates distortion and increases stability. **Omnitec Corp**, Phoenix, Ariz.
Circle 304 on Inquiry Card

Rotary Printed Circuit Switches

PC terminations on conventional rotaries, std/custom PCB assemblies, and flexible conductor cable switches are described in brochure which features diagrams and photos of PC and PCB switches. **Oak Industries, Inc, Switch Div**, Crystal Lake, Ill.
Circle 305 on Inquiry Card

DC Power Supplies

Catalog on 1- and 3ϕ, 500- to 10,000-W dc power supplies presents electrical specs, ratings, options, and prices on more than 75 models. **Electronic Measurements, Inc**, Neptune, NJ.
Circle 306 on Inquiry Card

Dial Backup for Online Networks

Brochure explaining how to reduce downtime caused by telephone line problems in large, real-time, online networks highlights dial backup equipment, which automatically switches remote sites to DDD network when private lines fail or become degraded. **Intertel, Inc**, Burlington, Mass.
Circle 307 on Inquiry Card

Remote Serial Link

Bulletin describes RTP7420/30 remote serial link, a full-duplex, private-line communications system that allows any digital computer equipped with a 4-wire asynchronous serial port to communicate directly with computer-directed measurement/control equipment. **Computer Products, Inc**, Fort Lauderdale, Fla.
Circle 308 on Inquiry Card

Light-Pen Technology

To aid in interactive CRT display system design, light-pen literature describes system basics, principles of operation, and factors influencing performance, such as luminous intensity sensitivity, spectral response, and phosphor emission characteristics. **Information Control Corp**, Los Angeles, Calif.
Circle 309 on Inquiry Card

Microcomputer Assembly-Language Reference Cards

Reference cards for use with the company's M and L series modular microcomputers are 6-page, pocket-sized folders which enable the programmer to compare machine codes against assembly language. **Conrol Logic, Inc**, Natick, Mass.
Circle 310 on Inquiry Card

IC Pluggable Packaging Assemblies

Catalog of wire-wrappable packaging boards, packaging sockets, and individual terminals includes modular, ECL, metric, and Schottky boards, along with adapters for LEDs, transistors, and alphanumeric displays plus ICs. **Garry Manufacturing Co**, New Brunswick, NJ.
Circle 311 on Inquiry Card

A-D Conversion Systems

Technical bulletin details price/performance tradeoffs of A-D conversion systems utilizing std building blocks that cover a wide range of requirements. **Tustin Electronics Co**, Santa Ana, Calif.
Circle 312 on Inquiry Card

Custom Power Supply Capabilities

Capabilities which include switching-regulated power supplies that use CMOS and special inhibiting circuitry for reliable operation and long life are discussed in bulletin. **Deltron, Inc**, North Wales, Pa.
Circle 313 on Inquiry Card

Power Supplies

Bulletin giving technical specs on seven series of single-output units and one series each of dual- and triple-output units includes features and illustrations. **Power Pac Inc**, Norwalk, Conn.
Circle 314 on Inquiry Card

4K RAM Pin-Outs

Pin-out configurations of the 4K RAM are discussed in applications study which covers package size, density, multiplexing, TTL and MOS clocks, output, and circuit design. **Intel Corp**, Santa Clara, Calif.
Circle 315 on Inquiry Card

Power Supplies

Catalog lists over 3000 std power supply modules with complete electrical specs, operating parameters, dimensional charts, and prices on from 1 through 99 pieces. **Abbott Transistor Laboratories, Inc**, Los Angeles, Calif.
Circle 316 on Inquiry Card

Miniature Toggle, Pushbutton Switches

52-page catalog discusses 1- through 4pdt "green" series, offering actuators with multiple actions, with choice of PC or solder lug terminals. **Alco Electronic Products, Inc**, North Andover, Mass.
Circle 317 on Inquiry Card

DC Power Supplies

Catalog on std power supplies and custom capabilities, plus electrical specs and prices, also details new product lines. **Power-One, Inc**, Camarillo, Calif.
Circle 318 on Inquiry Card

10-/16-Circuit Timer-Programmers

Bulletin describes Unistep border chaser models, and Varistep controllers whose circuit intervals are individually adjustable. **Bayside Timers, Inc**, Flushing, NY.
Circle 319 on Inquiry Card

Modular Test and Measurement Instruments

Catalog contains full specs on over 30 TM 500 plug-in modular instruments, data on mainframe power modules and accessories, and articles on applications of instrumentation to lab and industrial needs. **Tektronix, Inc,** Beaverton, Ore.
Circle 320 on Inquiry Card

Synchro Converters, Displays/Encoders

Catalog provides specs for 21 TTL-compatible products designed to satisfy any synchro/resolver or shaft interfacing requirements. **Computer Conversions Corp,** East Northport, NY.
Circle 321 on Inquiry Card

Digital Device Design

Engineering-aid handbook includes applications where digital-difference-to-analog (DD-A) converters serve as the interface between command and feedback digital quantities, as well as the analog power components of the system. **Computer Central,** Gaithersburg, Md.
Circle 322 on Inquiry Card

MOS Products

Microprocessors, memories, plus communication, watch, clock, calculator, and organ circuits, and liquid crystal displays as well as application notes are listed in catalog. **American Microsystems, Inc,** Santa Clara, Calif.
Circle 323 on Inquiry Card

Precision Magnetic Electro-Optical Components

Brochure discusses company's capabilities in terms of engineering, manufacturing, applications, quality control, and products. **Display Components Inc,** Littleton, Mass.
Circle 324 on Inquiry Card

Crystals, Oscillators, Filters, Delay Lines

Brochure listing over 40 quartz crystals, crystal oscillators, crystal filters, and solid ultrasonic delay lines includes frequency ranges/tolerances, temp ranges, drive levels, applications data, and performance guidelines. **Bliley Electric Co,** Erie, Pa.
Circle 325 on Inquiry Card

Test Sockets for Leadless Ceramic MiniChips

Data sheet illustrates and describes 6040-series sockets which accommodate 18- through 56-pad leadless ceramic circuits and occupy 1 sq in. **Azimuth Electronics,** San Clemente, Calif.
Circle 326 on Inquiry Card

45-, 55-Char/s Printers

Booklet gives complete specs for Sprint 45 and 55 daisywheel, bidirectional printers, including paper size, fonts, horizontal/vertical formats, ribbon types, and operator controls. **Qume Corp,** Hayward, Calif.
Circle 327 on Inquiry Card

Control Components

Catalog on control components, electromechanical assemblies, and indicators discusses essential functions, performance characteristics, and features. **Vernitron Control Components, a div of Vernitron Corp,** Torrance, Calif.
Circle 328 on Inquiry Card

Digital Printer

Series 7480 multi-line digital printer that records information from analytical and test instruments, production recording, weighing systems, process control monitoring, and data acquisition terminals is described in bulletin. **Veeder-Root, Digital Systems Div,** Hartford, Conn.
Circle 329 on Inquiry Card

Ceramic Capacitors

Complete line of ceramic disc and tubular feedthrough capacitors, with values from 0.75 pF to 2.2 μF and voltages from 3 to 6000 Vdc, is described in catalog. **Centralab Electronics Div, Globe-Union Inc,** Milwaukee, Wis.
Circle 330 on Inquiry Card

Executive Telecommunication Planning

Telecommunications systems planning manual offers common carrier rates, traffic tables, interface standards, and other practical reference material in single-volume, loose-leaf format. Updated monthly, annual subscription is $175 plus postage. **Center for Communications Management, Inc,** PO Box 324, Ramsey, NJ 07446.

Magnetic Bubble Technology

712-page book of selected reprints—a detailed appraisal of bubble technology and its applications for digital data storage and processing—is available at $11.95 (paperbound, IEEE members) or $23.95 (clothbound, $17.95 for members). Order postpaid from **IEEE Service Center,** 445 Hoes Lane, Piscataway, NJ 08854.

PC Design Template Set

Template set has been updated to include additional, frequently used component packages and mounting patterns for PC layouts and assembly drawings; patterns conform to MIL-STD-275C and IPC CM-770. Prices range from $12 to $20/set. **Tangent Template, Inc,** PO Box 20704, San Diego, CA 92120.

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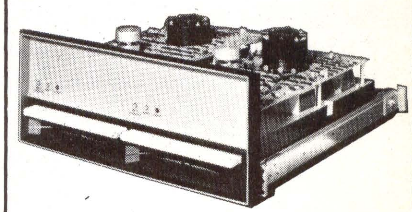

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GUIDE TO PRODUCT INFORMATION

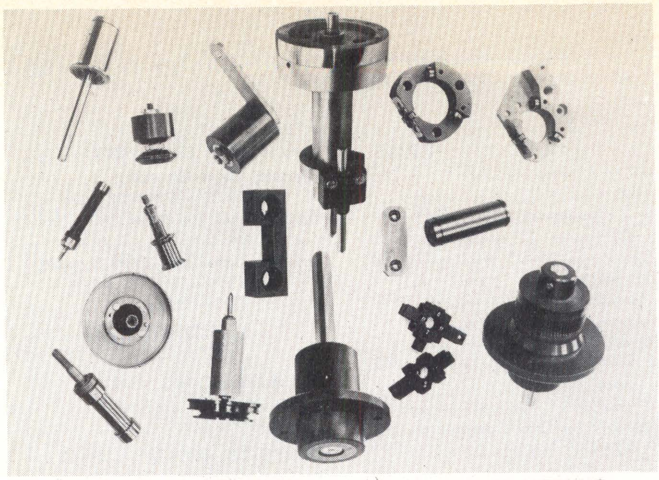
NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

MEMORY/STORAGE EQUIPMENT

INPUT/OUTPUT AND RELATED EQUIPMENT

COMPUTERS AND COMPUTER SYSTEMS

DATA COMMUNICATIONS EQUIPMENT



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New Hampshire Ball Bearings' ROTASSEMBLY Division has had many years of experience producing precision rotating and stationary components for a variety of customers. The product line includes tape guides, gimbal assemblies, pinch and feed rollers, precision idlers, fuel controls, capstans, motor encoders, miniature precision components for the data processing industry, guides, pulleys, and linear bearings. Each new product is thoroughly engineered to the design specification of the customer and submitted to him for his approval.

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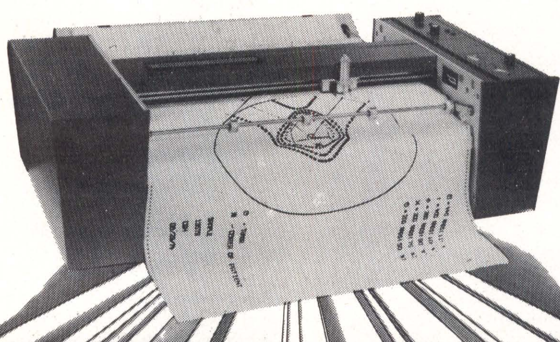

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ADVERTISERS' INDEX

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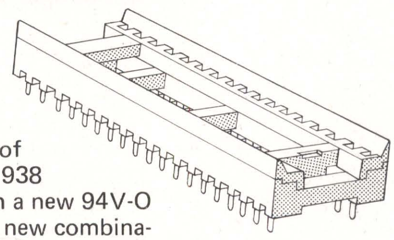
Molex would like you to test their new connectors last.

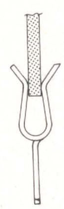
YES, LAST! After you evaluate our competition and then compare our new Closed Entry LSI Socket and Dual Edge Connector you will value the new innovations developed by Molex Affordable Technology.

CLOSED ENTRY LSI SOCKET
6097 SERIES



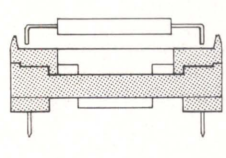
Description:
The 6097 Closed Entry LSI Socket combines the time-tested quality of the Molex Soldercon™1938 Dual Beam contact with a new 94V-O polyester housing. This new combination allows insertion and withdrawal of fragile LSIs without damage while maintaining sufficient normal force for a reliable low-lever electrical contact.

Key Features:



The Molex Soldercon™ features side bearing contacts. These contacts offer better overall contact reliability, mechanically, and electrically, because we are making contact with the main surface of the lead frame. Contact resistance remains constant after many insertions and withdrawals.

The 94V-O black housing design incorporates many desirable features such as the closed entry cap ... a tapered lead-in ramp to insure positive positioning of the LSI in the contact areas, and a closed socket base to prevent solder wicking during wave soldering.



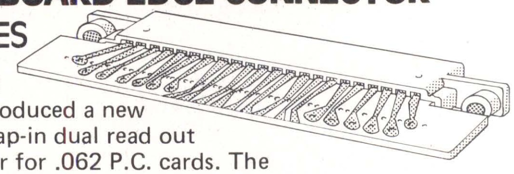
Options:
The 6097 is available in 24, 28, and 40 positions on .100 x .600 spacing. Contact platings and materials are available in tin, selective gold, and overall gold over brass or phos bronze material.

Economy:
The 6097-N could be the answer to your socketing headaches at a very competitive price. For example, a 24 position socket at the 5,000 piece level costs 24¢ each in tin.

Molex Service:
Molex has a nationwide network of representatives and distributors to handle your off-the-shelf and large quantity orders. Field engineers are at your service to solve your tooling problems.

Literature:
For your FREE 16-page Switch catalog including photos, line drawings and specifications of the Molex line, call (312) 969-4550; or write Molex Incorporated, 2222 Wellington Ct., Lisle, IL 60532.

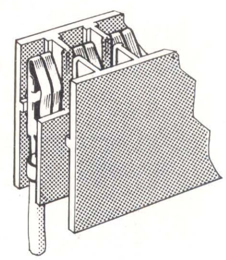
DUALCON™
DUAL P.C. BOARD EDGE CONNECTOR
4338 SERIES



Description:
Molex has introduced a new .156 crimp/snap-in dual read out edge connector for .062 P.C. cards. The crimp snap-in type contact allows greater production flexibility and at the same time reduces labor/assembly man-hours, **because you use only the contacts you need.**

Key Features:
The black polyester housing is dimensionally stable and requires no mounting panel revisions to replace most of the currently available edge-connectors of the solder loop or P.C./wire wrap type. The superior contact design features include an anti-overstress mechanism, bifurcated contact beam, coined contact edges, and an "anti-fish hooking" device to prevent tangling on the assembly line, and a built-in wire stop to prevent over stripped leads from interfering in the working area of the contact. The Dualcon™ Connector also meets—or exceeds—the applicable sections of MIL.C-21097.

Options:
The 5 Amp rated terminals are available with pre-tin gold over nickel, or selective gold plating and will accommodate 18–24, and 24–30 AWG. Solder loop and split eyelet type terminals are available. Inter-contact and on-contact polarizing keys are optional.



The connector housing is available with or without mounting flanges in 8, 10, 12, 15, 18, 22, 25, and 28 dual row positions.

Application tooling is available for hand termination, semi-automatic bench machines (available on lease or purchase terms) and fully automatic units for extremely high speed production.

Economy:
The Molex Dualcon™ system provides substantial savings on labor, as well as piece-part cost, for a totally reliable and economical inter-connect system. For example, the 15 position Dual Housing in 1,000 piece quantity fully loaded with 30,000 tin contacts in chain form would cost .91¢ each, (less than that if you do not require all positions loaded).

Save the best for last!

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